Software and Hardware Task Scheduling for FPGA-based Architectures

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**Context and Problem Statement**

FPGA circuits offer partial dynamic reconfiguration capabilities which allow them to perform spatial and temporal multiplexing of both hardware and software tasks. These properties make FPGAs suitable to implement embedded, dynamic, and highly parallel multi-tasked applications. Thus, they provide the best architectural trade-off between general purpose and flexible solutions based on processors, and high-performance systems based on ASICs or GPUs, as well as, the best trade-off between consumption and time-to-solution. Temporal partitioning of tasks as a function of the computational workload requires to develop a new dedicated middleware. Indeed, FPGA scheduling is made much more complex than single or multi processor scheduling due to the degrees of freedom the circuit offers. Such complexity is heightened in the context of a multi-FPGA computational substrate. Hence, it gets closer of a heterogeneous multi-processor scheduling, which vary continuously in both time and space. In the context of electrical autonomous vehicles, it becomes paramount to optimize the computational substrate consumption according to the given situations (i.e., variable computational workload as a function of the information stream). As a result, scheduling must be done online, as opposed to offline scheduling, where the application flow is known beforehand. Optimal scheduling may be computed before startup. However, in an online context [10], tasks finish times, as well as their duration are unpredictable; scheduling is then recomputed online according to events that occurred, e.g., arrival or end of a task, ...

Numerous works studied scheduling and real-time assignment for FPGAs [1, 2, 10, 11]. In [11], 1D and 2D online scheduling and real-time spurious tasks are posed, while the study performed in [4] focuses on real-time scheduling, preemptive but offline and 1D of periodic tasks. In [1] multi-versioned tasks and spurious tasks are processed in an online context, 2D and non-preemptive. In a context where the computational workload may vary, the computational substrate must be able to answer to the demand and be scalable. It then becomes necessary to propose new methodologies for task scheduling and assignment on heterogeneous substrates (FPGA + multicore), in a 3D context, online, and non-preemptive.

**Application to Bio-inspired Navigation of the VEDECOM Autonomous Vehicle**

In the past few years, progress in developing autonomous vehicles has been accelerating, thanks to vehicle partial driving delegation, autonomous shuttles, driverless vans, etc. Their performance in highways and urban environments vary depending on which planning and navigation algorithms are being used. Animals are equipped with navigation capabilities which are both performant and able to adapt to a dynamic environment. As a result, bio-inspired models for autonomous vehicles represent a promising exploratory track when considering their characteristics. Starting from a neurobiologically plausible model of the interactions of different cortical and subcortical structures of mammalian brains performing a navigation task, we propose a new control architecture for autonomous car. This neuronal architecture aims at replicating the underpinning neuronal mechanisms subtending the cognitive abilities involved in navigation (ranging from multi-modal perception, sensorimotor coupling to action selection). Sensory-motor learning is per-
formed on-line and built through the interactions with the environment (physical and social) [3]. Sensory information stemming from different sensors can then be learned and recognized by cells in the hippocampus, which can answer very locally in the environment, i.e., they are location cells. These cells are learned by extracting visual landmark from the environment and, combined with directions information (obtained using a magnetic or visual compass) as well as path integration, allow to characterize the current location [5–9]. This model’s scalability on large distances involves the increase of the number of learned locations, which induces issues of combinatory explosion, e.g., computational and memory overheads. Hence, long distance navigation requires us to redefine optimization strategies (sensory signals evaluation, taking the context into account during the learning phases, controlling the learning and adaptation phases, controlling the navigation strategies) [4], and an on-demand computational substrate.

With the support of the CNRS (national center for scientific research), the ETIS laboratory just developed (in March 2017) a unique board based on reconfigurable fabric. This board embeds nine heterogeneous circuits (Cortex A9 + Kintex 7) with a matrix topology $3 \times 3$. This computation plan thus allows to tackle issues tied to manycore heterogeneous architectures and programming models. These FPGAs are interconnected via a communication network through differential pairs, organized as a 2D mesh and from which digital communications can go through at a high rate between two neighboring routing nodes. The glue mapped to each FPGA allows for independent modification of both frequency and voltage, in order to reduce each circuit’s consumption, hence contributing to global consumption minimization.

**Objectives** This research will enable us to achieve the following goals:

- **OL** Design new scheduling and assignment methodologies for both hardware and software tasks on a 2D substrate, online, without preemption, all the while reducing consumption and guaranteeing a quality of service.
- **OL** Benchmark the implemented solutions on autonomous planning/navigation algorithms.
- **OL** Establish performance gains compared with architectures currently in use in the Védécom autonomous vehicle.

**Team**

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**References**


