Definition of an embedded reconfigurable matrix to improve energy efficiency of artificial neural networks

- **Deadline**: July 27, 2019
- **Career levels**: PhD student
- **Keywords**: Computer Architecture, Design Space Exploration, Energy Efficiency / Low-power Computing, Machine Learning / AI, Reconfigurable Computing

The goal of the PhD is to design next generations of logic matrix of eFPGA technologies in order to support the execution of Artificial Neural Networks and to improve the energy efficiency compared to classical implementation onto CPU or GPU.

Neural network implementation must face a dual challenge of computation intensive tasks and memory intensive tasks. To deal with this, the problem must be addressed both at the algorithmic level, where the complexity of the algorithm must be reduced by quantization and pruning steps, and at the hardware level, where it is possible to adapt computing and communication resources to the networks thus optimized.

In a SoC design perspective, embedded reconfigurable logic matrices can thus be adapted to better meet Artificial Neural Network (ANN) requirements. Multiple network models are studied in the literature: Convolutional, Binary, Spiking... And it will therefore be necessary to identify the most interesting model both from a technical point of view with regard to possible hardware developments, but also from an application point of view with regard to the fields requiring the design of dedicated SoC.

Based on this orientation on the ANN model, the objective will then be to determine the reconfigurable IP blocks necessary for their effective deployment on eFPGA matrix. The definition of specific computation blocks as well as specific memory blocks will be considered to support the best possible scalability.

The quality criteria of the solution thus developed will necessarily be evaluated according to surface area, performance and energy consumption, but more specifically to energy efficiency. This will be compared to standard implementations on embedded CPUs, GPUs and FPGAs with identical microelectronic technology.

This PhD is a tight collaboration between menta (https://www.menta-efpga.com/), a leading Tech company in the field of eFPGA, and University of Côte d'Azur in the heart of the Sophia Antipolis technopole. The PhD will be hosted at menta and should start in October 2019.