Implementation of a Soft-Core in FPGA Based on RISC-V ISA for Real-Time Interfacing and Control

- **Deadline:** Sept. 30, 2018
- **Career levels:** PhD student
- **Keywords:** Computer Architecture, Embedded / Cyber-Physical Systems, Runtime performance / Optimisation, Simulation

Description

Implement and optimize a soft-core in a FPGA based on RISC-V ISA. The core is targeted to be use to build easily and efficiently custom real-time protocol interfaces or control modules.

The intern will have the opportunity to work on many aspects of processor design and development. The internship will involve work on instruction-set simulators in C, assembly and compilation tools. It will also provide the opportunity to work on the implementation of the architecture in HDL and on simulation, synthesis and implementation in FPGA. It will require to perform tests for validation, performance assessment and optimization.

About ECS: Embedded Computing Specialists SPRL (ECS) is based in Brussels providing engineering services and solutions for R&D; in embedded computing. You’ll find more information about ECS on its website (http://www.ecspec.com/) or in the HIPEAC info newsletter n°48 (cf. https://www.hipeac.net/assets/public/publications/newsletter/hipeacinfo48.pdf#page=26)

Timing

The internship duration is 3 months, to be finished before mid December 2018.

Location

Brussels, Belgium

To apply please get in contact with Philippe Manet (philippe.manet(at)ecspec.com)