

HiPEAC

COMPILATION ARCHITECTURE

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**NETWORK OF EXCELLENCE ON
HIGH PERFORMANCE AND EMBEDDED
ARCHITECTURE AND COMPILATION**

**WELCOME
TO ACACES'14,
13-19 JULY 2014,
FIUGGI, ITALY**



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AUTUMN COMPUTING SYSTEMS WEEK, 8-10 OCTOBER 2014, ATHENS, GREECE

MESSAGE FROM THE HIPEAC COORDINATOR



In May, Google presented a prototype of the self-driving car that it wants to start testing by the end of the year. The car no longer has a steering wheel – which is quite a statement. Around the same time, Volvo started the biggest self-driving car experiment in Europe with 100 self-driving cars on 50 km of roads in the city of Gothenburg. I was surprised that the technology is apparently mature enough to do large-scale experiments in an urban environment. I was happy to learn that Europe is also active in this area.

I strongly believe that when the self-driving car will hit the market, it is going to completely change the way we think about mobility: no more need to have a driving license (even kids can use the car, some parents will for sure consider it safer than a bike), drinking and driving are no longer forbidden, traffic signs for cars are no longer needed, no more violations of traffic laws, ... I believe that the first killer application might be commercial long haul road transportation. Highways are a pretty predictable environment with only

cars and other vehicles, and truckers are expensive, they have to respect driving, break and rest times, and they are often the cause of accidents. There is a clear business case for self-driving trucks running 24/7. No doubt that taxis will follow, as will the general public. Given that fact that an average family spends more money on cars than on mobile gadgets, we are talking about a huge market.

In May, we celebrated 10 years of HiPEAC as part of the largest computing systems week ever organized by HiPEAC. The event was attended by 400 people from the European computing systems community. I was particularly pleased by the fact that several of the early HiPEAC pioneers joined us in Barcelona for the celebrations. Together we looked back at the accomplishments of the three HiPEAC projects, and we dreamt about the future.

In May, we passed a review of HiPEAC. The reviewers congratulated the network with the results, in particular with the increased

impact of the HiPEAC conference, the quality of the HiPEAC roadmap, and several other activities. They encouraged HiPEAC to look back and investigate which tasks from the last 10 years resulted in the highest measurable impact in the community, and to increasingly focus on these tasks in the future.

This newsletter is the summer school issue. The summer school also marks the beginning of the summer break for me. I wish you a relaxing summer with your family and friends, and I hope to see you again after the summer holiday in good health, and full of plans for the year to come.

Take care,
Koen De Bosschere

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Cover photography of Fiuggi by Matthias Jung



MESSAGE FROM THE PROJECT OFFICER

A few months ago I was asked to take responsibility of HiPEAC for the European Commission—a new adventure was starting! The first real contact that I had with the HiPEAC community was at the Vienna conference in January, and I was very favorably impressed by the high scientific quality of the work presented. Also, it was clear that the conference was a lot more than a set of lessons: the networking area was very busy, and informal contacts were going on at full steam. This is something that European scientific and industrial communities need very much: science is based on the circulation of ideas and people, and Europe cannot afford to have researchers working alone. HiPEAC fits very well in today's world of “connected research”, where the connection is not broadband, but person-to-person and idea-to-idea.

In HiPEAC I have seen a community of people working hard to improve their scientific know-how and academic recognition. This is definitely good, because Europe needs excellent research, which

has always been one of the high level objectives of Framework Programme 7. Moreover, good research institutions and universities have a significant economic impact, because they become catalysts for skilled people and investments.

But this is not enough: the new Framework Programme Horizon 2020 is defined as “a means to drive economic growth and create jobs” (<http://ec.europa.eu/programmes/horizon2020/en/what-horizon-2020>); this means that indirect impact, as we are used to, is no longer enough. What the European Union is asking us to do, today, is develop research and technology which is not only excellent, but which also has a direct and measurable economic impact. On the one hand this may be difficult, because a good scientist is not necessarily good in business; but on the other hand it is easy for the HiPEAC community, because the advanced computing technologies that you master have many very practical and very valuable applications, which are only going to increase in importance and value in the near future.

Recently we had, in parallel with the celebrations for the 10 years of HiPEAC, an important event hosted by the Barcelona Supercomputing Center and in line with this new direction of European research.

We called it the “impact workshop”, and it was the opportunity to bring together many projects working on several aspects of advanced computing, to assess and optimize their potential impact. We got very interesting results, which we are consolidating and will be published shortly, and which will guide the European Commission towards improving the impact of scientific work.

In conclusion, HiPEAC now faces a challenge: it has done a highly important and useful job for 10 years, but now the community must be able to take on board new challenges, in order to support scientists not only in their research activities, but also in optimizing the impact of their work. It is time to reflect on what HiPEAC should become: on the one side, European computing research needs a thriving scientific community, and on the other side, European industry also needs a reliable partner in order to get access to high-level talent, know-how and innovative technologies. Combining the best of these two worlds may be the key for a successful future.

Sandro D'Elia



Fiuggi by Matthias Jung

HIPEAC SPRING COMPUTING SYSTEMS WEEK, BARCELONA

This CSW featured a program with seven thematic sessions and the HiPEAC 10th Anniversary Workshop.

The program of the Spring Computing Systems Week held in Barcelona (May 13-15, 2014) consisted of seven thematic sessions. They resulted from a call issued last February. Before presenting a short summary of each of the sessions, I would like to acknowledge the organizers for their enthusiasm in preparing them and for their contributions to this summary for the HiPEAC Newsletter. Additional details about the presentations, and abstracts for most of them, are available at the HiPEAC website.

The following thematic sessions were organized:

HIPEAC ROADMAP 2015

HiPEAC develops a bi-annual roadmap. The 2015 version must be ready by the end of 2014, because it will be used as input for the Horizon 2020 calls in 2016/2017, leading to research activities in the period 2017-2021, and commercial exploitation in the 2020-2025 time frame. Hence, the challenge is to try to find out today what will be important ten years from now! The roadmap is a community document, which means that it builds on the insights of the members of the community.

This session, organized by Marc Duranton, from CEA, allowed all participants to share their vision about the future of computing in Europe. It focused on technologies, ideas, societal context, technologies (disruptive or not) etc. that could (or will) have an impact in 2020 and beyond, and it covered all technologies related to HiPEAC (hardware, software, systems, HPC, data servers, embedded...).

STREAMING APPLICATIONS FOR PARALLEL HARDWARE

The thematic session on streaming applications for parallel hardware, organized by Johan Eker (Ericsson), contained three technical talks. Jorn Janneck from Lund University started by laying the groundwork with a presentation on fundamental dataflow theory and introducing the CAL actor language. Mickaël Raulet from INSA presented tools for analysing and compiling CAL dataflow programs to manycore systems. Finally, Professor Marco Mattavelli from EPFL presented tools for synthesising dataflow programs to FPGA, including support for design space exploration. He also gave an overview of the MPEG standard based on CAL and dataflow.

DYNAMIC CO-OPTIMIZATION OF APPLICATIONS AND RESOURCE MANAGEMENT

Dynamic co-optimization of applications and resource management is an important issue for future HPC systems which may be best utilized by running multiple applications in a coordinated fashion on the same hardware. For increased flexibility and efficiency, applications could support resource management by providing hints and appropriately reacting to notifications on scheduling decisions.

To make the HiPEAC community aware of the importance of this

topic, as well as to trigger further collaborations, Michael Gerndt and Josef Weidendorfer from Technische Universität München (TUM), organized a corresponding thematic session at CSW in Barcelona. Both are involved in German national projects where co-scheduling is the focus of research, the DFG-funded TCRC89 "Invasive Computing" (<http://invasic.informatik.uni-erlangen.de/>) and the BMBF-funded project "FAST" (<http://www.fast-project.de/>), as well as in the European FP7 project AutoTune (<http://www.autotune-project.eu/>). The keynote by Joerg Henkel (Karlsruhe Institute of Technology), highlighted upcoming issues around dark silicon for resource management, and in the following, the just mentioned projects were presented to the audience.

Michael Glass (FAU Erlangen-Nuremberg) and Isaias Compres Urena (TUM) talked about InvasiC subprojects, and Jens Breitbart (TUM) discussed ongoing research in FAST. Further invited speakers were Eduardo Cesar (Universitat Autònoma de Barcelona), who presented auto-tuning techniques developed in the AutoTune project, as well as Raymond Namyst (University of Bordeaux), who talked about exploiting heterogeneous systems by composing multiple parallel libraries. The session finished with a panel moderated by Josef Weidendorfer about how much application involvement is needed for best resource management decisions. The event was well attended by around 50 international EU researchers, enriching the session with quite some interactivity and discussions.

IS CURRENT RESEARCH ON HETEROGENEOUS HPC PLATFORMS IN LINE WITH REAL-WORLD APPLICATION NEEDS?

This session debated whether current research on heterogeneous systems is actually in line with the demands of users of such systems. It was organized by Marisa Gil (BSC/UPC) and Chris Fensch (University of Edinburgh). The session was split into two parts. In the first half, two users of heterogeneous systems presented their experience from using their systems, and discussed what they see as the most critical issues that need to be addressed by the research community.

Pooyan Dadvand from CIMNE/UPC presented Kratos, an open source framework for developing parallel multi-physics programs to solve engineering calculations. Kratos has evolved over several years, from a sequential framework to one with GPU support. However, support for heterogeneous platforms is slowed by many real-world difficulties, such as the requirement to rewrite code (again and again!), lack of debugging support, external library dependencies, and sometimes too much pain for only modest gains.

Ana Lucia Varbanescu from the University of Amsterdam presented her experience with real time sound raytracing. While the problem is extremely parallel, the individual tasks are highly imbalanced in terms of computational complexity. In order to achieve the best performance, it is necessary to distribute the



work between CPU and GPU. As an example, Ana presented the Glinda framework, which performs such a static partitioning. The overall conclusion is that heterogeneous platforms have the potential to outperform homogeneous ones, but at the expense of increased development efforts. However, part of the efforts can be hidden in heterogeneous support libraries.

During the second half, a panel and the audience discussed the issues raised by Pooyan and Ana Lucia. On the panel were Grigori Fursin (Inria and leader of the discussion), Paolo Faraboschi (HP Labs), Ana Lucia Varbanescu, Mats Brorsson (KTH), Pooyan Dadvand, and Paul Keir (CodePlay). The panel felt that in about 80% of all cases these issues could be addressed with domain specific languages (DSL). The DSLs act as the interface between the framework developer/application programmer and the hardware expert. Application developers would be willing to rewrite their code using DSLs, as long as this remains the only time a code rewrite is required. However, a key concern seems to be the increasingly important issue of data partitioning, as HPC moves towards more irregular data structures. Overall, this requires better, simpler and agreed APIs for everyone to follow. The current abstractions, e.g. CUDA, OpenCL, OpenACC, are not suitable for this task. An interesting point was raised by Bilha Mendelson (independent consultant): how can we prevent the current situation, where software developers have to repeatedly update their code in response to the changing demands of hardware? The panel seemed quite pessimistic in this respect, as games software seems to be the only significant example of the converse, where software demands have driven developments in hardware. Another question the panel raised was whether it was possible to leverage cloud software development in a similar way

to mobile software distribution; something similar to an AppStore for HPC computing.

With 80 delegates, this session was the best attended so far in our series on heterogeneous systems and programming models.

MICROSERVICES AND VIRTUALIZATION

The session on microservices and virtualization was split into two slots. The first slot focused on low-power techniques for microservices. Microservices use a large number of lightweight computing nodes configured to share an infrastructure, including power, cooling fans, and I/O devices in a common chassis. Several classes of data center workloads, such as low-end dedicated hosting and content delivery, tend to scale well in such infrastructures. The first invited speaker, Antonios Motakis from Virtual Open Systems, introduced VFIO (Virtual Function I/O), a Linux kernel infrastructure, which takes advantage of the capabilities of modern IOMMUs to allow devices to be driven directly from user space, without a specialized kernel driver needing to be involved. Audience questions and participation showed a real interest in this novel Linux infrastructure and the possibilities for research on ARM-based environments. Next, Denis Dutoit from CEA, talked about the EUROSERVICES project and showed how 3D integration of chiplets onto an active interposer can enable low power and scalable computing components. He explained how interposer technology can be used to stack chips side-by-side, allowing designers to put dies next to each other in a high-bandwidth, low-latency, low-power configuration. Answering questions, he explained that the main challenges of the new technology would be the TSVs and alignment of the chiplets on top of the interposer. Finally, John Goodacre from ARM

described the ARM technology focusing on Data Centers. He described the evolution of the ARM Architecture, as well as the ARM Virtualization Extensions, which will enable ARM-based microservers.

The second slot of the thematic session focused on three different aspects of virtualization technology. The first speaker was Michael Swift from the University of Madison-Wisconsin. He presented a new kind of attack on co-located virtual machines in the cloud called a "resource freeing attack". In this attack, co-located VMs are victimized and coerced into freeing up resources such as memory or CPU time. Professor Swift showed how a given VM can take advantage of the freed resources to increase performance. The second speaker was Juan Quintela, from the virtualization team at Red Hat. He spoke about Red Hat's progress in live VM migration, and how the same techniques can be applied to enable fault tolerance. Juan explained that the main advantage is the ability to implement VM-level fault tolerance on commodity hardware. The final speaker was Joel Nider from the virtualization team at IBM Research. He presented some of IBM's latest work in I/O virtualization, in which a specialized server is used to interpose on the I/O for a set of machines hosting VMs. The specialized server enables I/O device consolidation at the rack scale for future data centers. Each speaker gave a short presentation, which left time at the end of the session for an open discussion among the attendees. The discussion invited a wide range of questions on various applications of virtualization technology, as well as future directions. The three speakers each offered their opinions on each question, which sparked responses and further questions from the audience.

CHALLENGES IN MIXED CRITICALITY AND REAL-TIME AND RELIABILITY IN NETWORKED COMPLEX EMBEDDED SYSTEMS

This thematic session was organized by Gerhard Fohler, University of Kaiserslautern, Jaume Abella, Barcelona Supercomputing Center, and Yanos Sazeides, University of Cyprus. The thematic session aimed at identifying specific demands and research issues in the areas of mixed criticality systems and combined real-time and reliability, and raising awareness of not fully understood application demands, research topics and challenges. With the EU FP7 projects DREAMS and PROXIMA as crystallisation points, it brought together representatives from related initiatives (HARPA, VeTeSS, CLERECO, PROARTIS, OMAC4S, RACE), and experts from both industrial applications and demands, as well as researchers in state-of-the-art and novel research directions. Special focus was given to understanding specific challenges from related application domains: avionics, automotive, and space, to identify what is actually meant by mixed criticality, and which problems should be solved. The session filled a full day.

Daniel Gracia Pérez (Thales Research & Technology) discussed mixed criticality issues in the avionics domain; Kai Höfig (Siemens AG) focussed on the automotive domain; and Hans-Jürgen Herpel (Airbus) talked about mixed criticality in the space domain. Giorgio Di Natale (Montpellier Laboratory of Informatics) presented the CLERECO project aiming at efficient evaluation of the reliability of future system designs; Carles Hernández (BSC) presented the benefits of light lockstep to timely detect errors with low cost; Damien Hardy (University of Rennes I / IRISA)

showed a method that statically calculates a probabilistic WCET bound in the presence of permanent faults in instruction caches; and George Klokarris (University of Cyprus) presented a model of how the performance is affected by permanent faults. William Fornaciari (Politecnico di Milano) presented the HARPA project, and the management of mixed-criticality and reliability at runtime; Tullio Vardanega (University of Padua) presented techniques for resource sharing in multicores; Francisco Cazorla (BSC) showed mechanisms for resource sharing and partitioning. Michael Zolda (University of Hertfordshire) presented methods for software development for cyber-physical systems; Jon Pérez (Ikerlan) presented modular certification; and Roman Obermaisser (University of Siegen) presented techniques for integrating different models of computation.

The session was well attended and of a strongly interactive nature, underlining interest in the areas and liveliness of the related research areas. It achieved high cross dissemination by bringing together related, but not closely linked research communities, as well as exposing the topics to the HiPEAC community at large. A webpage was set up to document the session for use in the community building activities of the DREAMS and PROXIMA projects.

THE CHALLENGES AND OPPORTUNITIES IN THE SPACE AHEAD OF RECONFIGURABLE COMPUTING

The session on reconfigurable computing was organized by Georgi Gaydadjiev (Chalmers University of Technology and TU Delft). It consisted of seven talks related to reconfigurable architectures and their potential.

Reiner Hartenstein (TU Kaiserslautern and Karlsruhe Institute of Technology) discussed the multiple dimensions available for design-space exploration on reconfigurable architectures. Dionisios Pnevmatikatos (FORTH-ICS and University of Crete) presented how partial reconfiguration can be used in FPGA devices. Daniel Jimenez (BSC/UPC) presented the OmpSs@Zynq approach, for accelerated kernels exploited in FPGA devices using the OmpSs programming model. Dimitrios Sourdis (Technical University of Athens) presented their work on a vision system targeting applications to be used in space. Georgi Gaydadjiev presented a 2D view of computer systems, with the aim of reducing programming complexity. Cristina Silvano (Politecnico di Milano) presented a method to manage adaptability of reconfigurable architectures through performance monitoring and prediction. And Per Karlstrom (Maxeler Technologies) showed the exploitation of dataflow engines in driving high-resolution monitors over DVI, in order to enable very low latency user experiences.

We expect HiPEAC members to continue organizing and participating in thematic sessions, as a good way to disseminate your research results and have interesting networking sessions. They are useful to promote research areas in the HiPEAC community, to share research results and to build a network of researchers from which new consortia for future project proposals can grow.

Xavier Martorell, Barcelona Supercomputing Center

EVENT REPORT: BOJAN FURLAN

The HiPEAC Spring Computing Systems Week was organized in Barcelona from 13 to 15 May 2014. Besides the thematic sessions, a very special event took place - the celebration of the 10 year anniversary of the Network of Excellence. This event was included the Anniversary Workshop, which was full of inspiring talks, with a number of high level keynotes, concluding with a pleasant festive dinner.

Among the many pearls of wisdom that I heard during this event, I would like to share one about sailing. The credit for the story goes to Mario Nemirovsky (BSC) from our chat. This is my free interpretation: if you are not leading and you want to win at the sailing race, what should you do? You should do anything except follow the leader. Because doing the same moves as the leader will keep you in the same order, behind the leader. If you are winning, what should you do to stay in first place? Well, the only thing you should do is to look behind you and do the same as the one that is approaching the fastest. So, if you are winning it can be easy; if not, you must be brave and creative. Don't (always) follow the leaders, (sometimes) choose your own path!

Bojan Furlan, University of Belgrade, Serbia



EVENT REPORT: ALGIRDAS LANČINSKAS



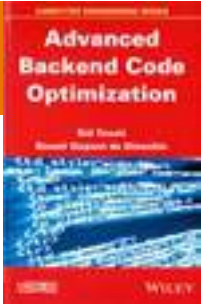
I am currently a researcher at the Institute of Mathematics and Informatics of Vilnius University, Lithuania. I would like to thank the HiPEAC Network of Excellence for giving me the opportunity to take part in the HiPEAC Spring Computing Systems Week, which was held in Barcelona in May 2014. It was the first Computing Systems Week I ever attended and I have realized that it is a good chance for researchers and PhD students to gain valuable experience and keep in touch with the community of researchers in the field of high performance computing.

Participation in the event provided an opportunity to listen to interesting presentations, which gave me valuable knowledge and insights that will undoubtedly benefit my current research in the solution of complex optimization problems using high performance computing systems. I was very satisfied by the talks given in the thematic sessions "Streaming Applications for Parallel Hardware" (organized by Johan Eker), "Is Current Research on Heterogeneous HPC Platforms in line with Real-world Application needs?" (organized by Marisa Gil and Chris Fensch), and "The Challenges and Opportunities in the Space ahead of Reconfigurable Computing" (organized by Georgi Gaydadjiev).

I was also honored to participate in the HiPEAC 10th Anniversary Workshop, orga-

nized as a part of the Computing Systems Week, and to listen to the inspiring talks given by the honorable invited speakers. Finally, I would like to thank the organizers for the memorable (at least for me) scientific event and the pleasant environment for communication with colleagues during the coffee breaks and lunch times, as well as for getting informative feedback on any question regarding the participation in the event. I believe that this was not the last Computing Systems Week I will participate in, and I look forward to participating in forthcoming events.

*Algirdas Lančinskas,
Institute of Mathematics and Informatics
of Vilnius University, Lithuania*



BOOK: ADVANCED BACKEND CODE OPTIMIZATION

A summary of more than a decade of research in the area of backend code optimization for high performance and embedded computing, this book contains the latest fundamental and technical research results in this field at an advanced level. With chapters on phase ordering in optimizing compilation, register saturation in instruction level parallelism, code size reduction for software pipelining, memory hierarchy effects in instruction level parallelism, and rigorous statistical performance analysis, it covers material not previously covered by books in the field. Other chapters provide the latest research results in well-known topics such as instruction scheduling and

its relationship with machine scheduling theory, register demands, software pipelining and periodic register allocation. As such, Advanced Backend Code Optimization is particularly appropriate for researchers, professors and high-level Master's students in computer science, as well as computer science engineers.

AUTHORS INFORMATION

Prof Sid TOUATI is currently a professor at University Nice Sophia Antipolis in France. He was a former associate professor at the University of Versailles Saint-Quentin en Yvelines. His research interests include code optimization and analysis for high performance and embedded processors, compilation and code generation, parallelism, statistics and performance

optimization. He completed his habilitation thesis on backend code optimization, his PhD thesis on register optimization, and he has a master diploma in computer science. His research activities are conducted at Institut National de Recherche en Informatique et Automatique (INRIA) as well as in Centre National de Recherche Scientifique (CNRS).

Dr Benoit DUPONT de DINECHIN is currently Chief Technology Officer at Kalray (France). He was previously a researcher and engineer at STMicroelectronics in the topic of backend code optimization in the advanced compilation team. He has a PhD in computer science, in the topic of instruction scheduling for instruction level parallelism, and a computer engineering diploma.



BOOK: ROUTING ALGORITHMS IN NETWORK-ON-CHIP

A unified platform for building the basis of routing algorithms in NoC architectures

As technology geometries have shrunk to the deep sub-micron regime, the communication delay and power consumption of global interconnections in high performance Multi-Processor Systems-on-Chip (MPSoCs) are becoming a major bottleneck. The Network-on-Chip (NoC) design paradigm, based on a modular packet-switched mechanism, can address many of the on-chip communication issues such as the performance limitations of long interconnects, and the integration of a large number of Processing Elements (PEs) on a chip. The overall performance of a network depends on several network properties such as topology, routing algorithm, flow control and switching technique. The routing algorithm, in particular, has a strong impact on several non-functional

requirements of a NoC based system. Performance, reliability, energy consumption, power dissipation, thermal aspects, and fault tolerance, represent just a short list of the main common metrics affected by the routing algorithm. The scientific literature related to NoC architectures and design methodologies is mostly dominated by works addressing issues concerning the routing algorithms. Unfortunately, although the topic is so important and so widely discussed in the NoC community, there is a lack of structured resources (i.e., books, monographs, etc.) aimed at organizing the great deal of literature and information on routing algorithms used in NoC based systems. The goal of Routing Algorithms in Networks-on-Chip is to provide a unified platform for student (Master, PhD), researchers (from both academia and industry), and practitioners, for building

the basis of routing algorithms for NoCs as well as providing in-depth discussions on advanced solutions (applied and to be applied) in current and next generation NoC-based many core SoCs. After a basic introduction on the NoC design paradigm and architectures, routing algorithms for NoC architectures are presented and discussed at all abstraction levels: starting from the algorithmic level to their actual circuitual implementation. The impact on current and future key design objectives, namely power dissipation, energy consumption, thermal aspects, reliability, and performance is analysed and discussed.

Maurizio Palesi and Masoud Daneshtalab, Kore University, Italy and University of Turku, Finland

EUROPEAN LLVM CONFERENCE 2014

Europe's largest open-source compiler conference brings together industry and HiPEAC members

The fourth European LLVM conference (EuroLLVM) took place from April 7 to 8 in Edinburgh. After previous events in London and Paris, the conference was held for the first time in Scotland's capital. It attracted over 200 attendees from industry, academia, and the open-source community from Europe, the US, and Asia. The conference programme included two keynote speeches, fourteen technical presentations in two parallel tracks, two hands-on tutorials, ten lightning talks, a number of posters, and ample time for networking between participants during an informal "Hackers' Lab" and a conference gala dinner. The content presented at the conference has been published on the conference website. Celebrating 10 years (last year) since the release of version 1.0, LLVM has become one of the most widely used compiler frameworks and is backed by a vibrant open-source community that includes contributors from major industry players, as well as academia and hobbyists. With Clang, the project provides one of the leading C/C++ compilers and the first to fully implement the new C++11 standard. It forms the basis for a wide range of industrial products and academic research projects, with over 1000 publications citing LLVM. The LLVM Foundation, a non-profit entity to coordinate the project, has recently launched in the US and is hoped to further strengthen the growing community. The EuroLLVM conference serves as a venue to discuss recent innovations and hot topics around the LLVM project. In the first keynote, Chandler Carruth (Google) discussed the current optimization pass manager, its shortcomings, and his ongoing work to improve

it. Marshall Clow (Qualcomm) used his keynote speech to give the audience a taster of the upcoming C++14 standard and future developments in the ISO C++ standardization process. The technical presentations covered many different aspects of LLVM development and its use in various domains. These included a talk by the Sony compiler team about the recently launched LLVM-based compiler toolchain for the PlayStation 4; the presentation of Google's Portable Native Client project; a talk about the new little-endian PowerPC ABI developed by IBM; and the launch of a Clang-based frontend for the icc compiler by Intel. Two hands-on tutorials, one on backend development, another on automating large-scale code refactoring, gave participants a chance to learn about these important use cases from experts in the field. Posters and lightning talks complemented the talks and gave the audience an impression of the diverse projects that make up the LLVM ecosystem. In addition to technical presentations, the EuroLLVM conference was also an opportunity for members of the community to meet and network in person. For an open-source project with collaborators and users spread across countries and continents, such occasional face-to-face interaction is crucial. Due to the high amount of industry participation (>60% of attendees), the conference also fosters the exchange of ideas between industry and academia and serves as a recruitment opportunity for skilled engineers and researchers. The many lively discussions during the coffee breaks, the Hackers' Lab, and the gala dinner at the National Museum of Scotland attest to



the importance and success of this aspect of EuroLLVM. Tobias Edler von Koch, who organised the conference alongside colleagues from the University of Edinburgh and the LLVM community, was especially thankful for the support of the many industrial sponsors: "EuroLLVM 2014 would not have been possible without the generous financial support from ARM, Qualcomm, Codeplay, HSA Foundation, Google, and Parrot." With overwhelmingly positive feedback from participants, the event was a great success. "The level of attendance and the quality of the presentations reflect the impressive strength of the LLVM community in Europe, which continues to grow every year", says Philippe Robin, Director Open Source at ARM. Planning is already under way for the next iteration of EuroLLVM, to take place in 2015. To view the conference programme and presentation slides, visit <http://llvm.org/devmtg/2014-04/>

Björn Franke, University of Edinburgh, United Kingdom

PER STENSTRÖM ELECTED AS MEMBER-AT-LARGE OF THE ACM COUNCIL

Prof. Stenström from Chalmers University of Technology in Gothenburg, Sweden has been elected for a four-year term as Member-at-Large of the ACM Council. This follows the results of this year's election in

which also Alexander L. Wolf, Imperial College, London, was elected as ACM President for a two-year term. The new officers elected by ACM professional members represent the more than

100,000 computing professionals and students who comprise ACM's international membership.

THE GAUSS BEST PAPER AWARD FOR IBM RESEARCH ZURICH AND TUDELFT-COMPUTER ENGINEERING AT THE INTERNATIONAL SUPERCOMPUTING CONFERENCE

The paper 'Exascale Radio Astronomy: Can We Ride the Technology Wave?' written by Erik Vermij, IBM Research and PhD student at the CE lab-TU Delft, Leandro Fiorin, IBM Research, Christoph Hagleitner, IBM Research, and Koen Bertels, Delft University of Technology has been awarded the Gauss Award at the 2014 International Supercomputing Conference which will

take place in Leipzig from June 22 to 26. The Gauss Award is sponsored by the German Gauss Center for Supercomputing, which is a cooperation of the German national supercomputing centers at Garching, Jülich and Stuttgart. The winner of the Gauss Award will receive a cash prize of 3,000 Euro, courtesy of the German Gauss Center for Supercomputing.

Erik Vermij, IBM Research and PhD student at the CE lab at TU Delft, Leandro Fiorin, IBM Research, Christoph Hagleitner, IBM Research, and Koen Bertels, Delft University of Technology, Netherlands and Switzerland.

FAST PARALLEL PARSING OF REAL LANGUAGES IS NOW POSSIBLE – THE PAPAGENO GENERATOR TOOL

The parser generation tool PAPAGENO produces fast, parallel, deterministic parsers, which are implemented as multiple threads on standard multicore machines. Packaged as a replacement of the popular tool GNU Bison, our generator produces faster sequential parsers that at generation time can be configured into a specified set of parallel parsers, thus achieving almost linear speedup in a significant range of source program sizes and number of physical cores. The current release integrates parallel lexer implementations, based on GNU Flex, with the parallel parser, and attains larger speedups. The parsing algorithm is driven by a precedence table, uses one push-down stack per thread, and is produced starting

from a BNF grammar of the operator-precedence (OP) type. While most existing grammars, if not already fit for OP analysis, can be made into OP by small adjustments, other grammars (such as for the Lua language) can be recast into OP form by means of local transformations performed by the lexer. Parallel parsers and lexers for the JSON and Lua languages are included in the download. We are currently working on JavaScript. The parsers produced are encoded in standard C and use standard libraries. The tool source code is available at <https://github.com/PAPAGENO-devel/papageno> For more information, see [1,2]. Our team is interested in user experiences on parallel parsing and is open to collaboration. References

[1]. A. Barengi, S. Crespi Reghizzi, D. Mandrioli, F. Panella, and M. Pradella. The PAPAGENO parallel-parser generator. In *Compiler Construction 2014*, Grenoble, Lect. Notes Comput. Sci., pages 1-4. Springer, 2014.

[2]. A. Barengi, S. Crespi Reghizzi, D. Mandrioli, and M. Pradella. Parallel parsing of operator precedence grammars. *Inf. Process. Lett.*, 113(7):245–249, 2013.

Alessandro Barengi, Stefano Crespi Reghizzi, Dino Mandrioli, Federica Panella, Matteo Pradella, Dipartimento di Elettronica, Informazione e Bioingegneria - Politecnico di Milano

MIQUEL PERICÀS TAKES OVER ASSISTANT EDITOR ROLE FOR HIPEAC NEWSLETTER

Dr. Rubén Titos-Gil from Chalmers University of Technology has served as assistant editor, helping Prof. Per Stenström in his role of editor of the HiPEAC newsletter for the past two years. Rubén has recently moved on to a new position at

the Barcelona Supercomputing Center, and has left his role at the newsletter. Dr. Miquel Pericàs, a postdoctoral researcher at Chalmers University of Technology, will from now on be helping Prof. Stenström with this task. The HiPEAC community

wants to thank Rubén for his great work and welcomes Miquel to the Newsletter production team!

TU BERLIN PRESENTS A NEW VERSION OF ITS OPTIMIZED HEVC/H.265 DECODER

When combining performance optimizations and low-power modes it is possible to achieve low-power video decoding on mobile and desktop processors

TU Berlin is proud to present a new version of its highly efficient 4k Ultra High Definition (UHD) capable HEVC/H.265 decoder. A demo setup is created with a 65-inch Samsung UHD TV and a custom mini-PC based on the 4th generation Intel Core processor that includes the new Intel Iris Pro Graphics. Optimization for the latest generation processors allows the compact setup to decode UHD faster than 200 fps even at higher bit depths using four threads. UHD real-time operation (50 fps) is achieved for bitrates up to 20 Mbps using only two cores. With TU Berlin optimized decoder, and using commodity processors, it is possible now

to create low-cost, low-space, and relatively low-power UHD playback solutions. Because not all the cores are needed for video decoding, developers can use the remaining computing resources for other applications, or the unused capacity can be employed to improve power efficiency. The video decoder has been adapted for exploiting the low power modes available in mobile and desktop processors. The AES TU Berlin team is in the process of creating a spin-off for commercializing its high performance video coding solutions. The optimized HEVC/H.265 decoder is already available for licensing. More information can be found in the group webpage:



<http://hevc.aes.tu-berlin.de>

Mauricio Alvarez-Mesa, Chi Ching Chi, Ben Juurlink, TU Berlin, Germany

ARTEMIS: EMC² - EMBEDDED MULTI-CORE SYSTEMS FOR MIXED CRITICALITY APPLICATIONS IN DYNAMIC AND CHANGEABLE REAL-TIME ENVIRONMENTS

Start of ARTEMIS Project EMC² on April 1st

Born on April 1st 2014, the EMC² project is one of the largest ARTEMIS projects ever. The project originated from HiPEAC members and now totals 100 partners, HiPEAC and non-HiPEAC, from 19 different European countries. It crosses over multiple technologies, from the semiconductor industry, tool vendors, to application industries. The latter spans the range from automotive, avionics, and space, to industrial manufacturing, logistics, and the Internet of Things. About 800 person months are collectively invested by these partners, resulting in a tremendous innovation power, from both academia and industry.

EMC² targets the fading boundaries across application domains, where ubiquitous connectivity, interoperability, and product-line evolution drive the success of embedded and industrial automation systems. EMC² also addresses the challen-

ges and opportunities of multi-core and many-core computing platforms, with the promise of real breakthroughs for system and application integration, cost and energy efficiency, and performance. A major industrial challenge is posed by the cost-efficient integration of different applications with multiple levels of criticality regarding safety and security, on a single computing platform, in an open and evolutionary context.

The objective of the EMC² project is to foster these changes through an innovative and sustainable service-oriented architecture for mixed criticality applications in dynamic and changeable real-time environments. EMC² embraces the ARTEMIS strategic targets of reducing the cost of system design and development cycles by 15%, reducing the effort and time required for the revalidation and recertification of systems after implementing

such changes, also by 15%, and managing a complexity increase of 25% with 10% reduced effort. To meet these ambitious goals, EMC² consists of two groups of work packages, the technical work packages and the demonstrators, the so-called living labs. The six technical work packages address different levels of system architecture and development, from hardware to the software platform, as well as issues regarding system qualification, certification, and software maintenance. The developed approaches will be evaluated within six living labs, where each one focuses on a different application domain. The EMC² technology innovations combined with the results of previous European research projects are used in innovative ways to build a base for future embedded mixed-criticality multi-core applications. The project originated from a group around HiPEAC members Rafael Zalman and Knut Hufeld (both Infineon

IN THE SPOTLIGHT

Technologies AG), together with Sascha Uhrig (TU Dortmund), Marc Duranton (CEA), Albert Cohen (INRIA), Avi Mendelson (Technion) and Koen de Bosschere (Gent University). EMC² is coordinated by Infineon Technologies AG and most of the original members are still aboard. Coordi-

nation is supported by a large management team with work package leaders on the technical level and country coordinators on the political level. EMC² is receiving funding from the ARTEMIS Joint Undertaking and the national funding authorities under grant agreement no 621429.

Sascha Uhrig, Albert Cohen, Technical University of Dortmund, Germany; INRIA, France



FP7 ASPIRE PROJECT

Three leading digital security companies team up to bring strong software protection to mobile devices

- *In the fast moving space of smartphones and tablet computers, software-based security solutions offer a lot of benefits in terms of flexibility.*
- *Classical server-based licensing mechanisms are not applicable to mobile devices that are not always connected, and separate hardware modules like smartcards or dongles are not always compatible with the form factor of mobile devices.*
- *The ASPIRE project will develop strong software protection solutions that can be broadly applied to a wide range of application domains and that can provide security in environments where either no hardware-based security is available or as a complement to existing hardware-based security solutions.*

Ghent, April 17, 2014 – The massive adoption of mobile computing platforms creates an urgent need for secure application execution on such platforms. Unfortunately, today's mobile platforms do not support strong security solutions equivalent to set-top box smartcards or dongles to reliably control licensing terms. Furthermore, many of these mobile devices are shared by professional and private applications, and are thus intrinsically hard to control and secure.

Michael Zunke, chief technology officer of SafeNet's Software Monetization Business Unit states that "Security is ever more essential as an enabler for sustainable innovation of mobile applications and services. Security solutions based on custom hardware security components like dongles and smart cards are not a natural fit for these mobile environments. The industry therefore needs a comprehensive security framework in which software protection is the key ingredient." According to Brecht Wyseur, NAGRA's

security architect, the big challenge in the next years will be to increase the security level of software solutions to allow for both cost-effective deployment and long-term renewability, either stand-alone or in combination with a hardware root of trust.

Hence, more research is needed to come up with a solution that is strong enough to be viable for an increasing number of applications in which privacy and security are essential. The ASPIRE project will create the ASPIRE software security framework which will develop, combine and integrate five different types of software protection techniques into one easy to use framework. It will deliver comprehensive, effective security metrics and a decision support system to assist the software developer. "The integrated tool chain will allow service providers to automatically protect the assets in their mobile applications with the best local and network-based protection techniques," notes Bjorn De Sutter, coordinator of the project, adding

that "ASPIRE will make mobile software more trustworthy by leveraging the available network connection and by developing a layered security approach of strong protections. We will also make it measurable by developing practical, validated attack and protection models and practical metrics."

ABOUT ASPIRE

ASPIRE is an FP7 collaborative research project that brings together three market leaders in security ICT solutions. Gemalto

SA is the world leader in the smart card business. SafeNet is the world leader in software protection, licensing, and entitlement management, providing solutions to software companies globally. NAGRA, the digital TV division of the Kudelski Group (SIX:KUD.S), provides security and multiscreen user experience solutions for the monetization of digital media.

The project runs from November 2013 until October 2016, has a total budget of €4.6M, and has received funding from the

European Union Seventh Framework Programme (FP7/2007-2013) under grant agreement number 609734. It is coordinated by Ghent University. See also www.aspire-fp7.eu.

Bjorn De Sutter, Ghent University, Belgium



ERC PROJECT MECCA: FIRST RETREAT

Improving the design flow for parallel and heterogeneous architectures running real-time applications

Per Stenström's ERC project MECCA: Meeting the Challenges in Computer Architecture commenced in 2014 to deliver its ambitious goals. The MECCA project at Chalmers University of Technology promises to address three important challenges facing computer architecture: parallelism, power and predictability (the 3 P's). The project is already staffed with three exceptional and enthusiastic postdoctoral researchers: Risat Pathan, Miquel Pericàs, and Vassilis Papaefstathiou (another 3 P's). The process to recruit some excellent PhD students for the project is ongoing.

The first MECCA retreat took place on May 22 and 23 at the beautiful small island of Kåringön, 95 km northwest of Gothenburg. The event organizers were very happy to have Professor Yale Patt among the participants. Beyond the PI and the postdocs, the participant list also included adjunct professor Fredrik Dahlgren (Chalmers and Ericsson AB), associate professor Ioannis Sourdis, and PhD students Angelos Arelakis and Dmitry Knyagin.

The retreat has served to outline the participants' view on the most critical research questions concerning the project's three P's. Per presented his vision for MECCA, described the important challenges for computer architecture in the coming years, and set high goals for the project. Afterwards, everyone was excited to attend Yale's inspiring and thought-provoking talk about the future of computer architecture. Fredrik presented his view on future challenges for computing systems, blended with deep industrial insight. The project's postdocs presented research directions on the fields of their expertise and stimulated interesting discussions. The event was full of brainstorming sessions alternated with breaks for delicious seafood from the local archipelago. At the end everyone was full of new ideas and all agreed that it was a true success!

The MECCA project, Meeting the Challenges in Computer Architecture, is financed by the European Research Council through an Advanced Grant. The project officially started February 1st 2014, and the grant is for 2.3 million Euro over 5 years. Further openings for PhD studentships are expected in autumn, so prospective students should stay tuned in the HiPEAC and Chalmers websites.

Vassilis Papaefstathiou, Risat Pathan, Miquel Pericàs and Per Stenström, Chalmers University of Technology, Sweden



FP7 FASTCUDA: AN FPGA-BASED ACCELERATOR & HARDWARE-SOFTWARE CODESIGN TOOLSET FOR CUDA

Taking advantage of already-parallelized CUDA kernels in Hardware!

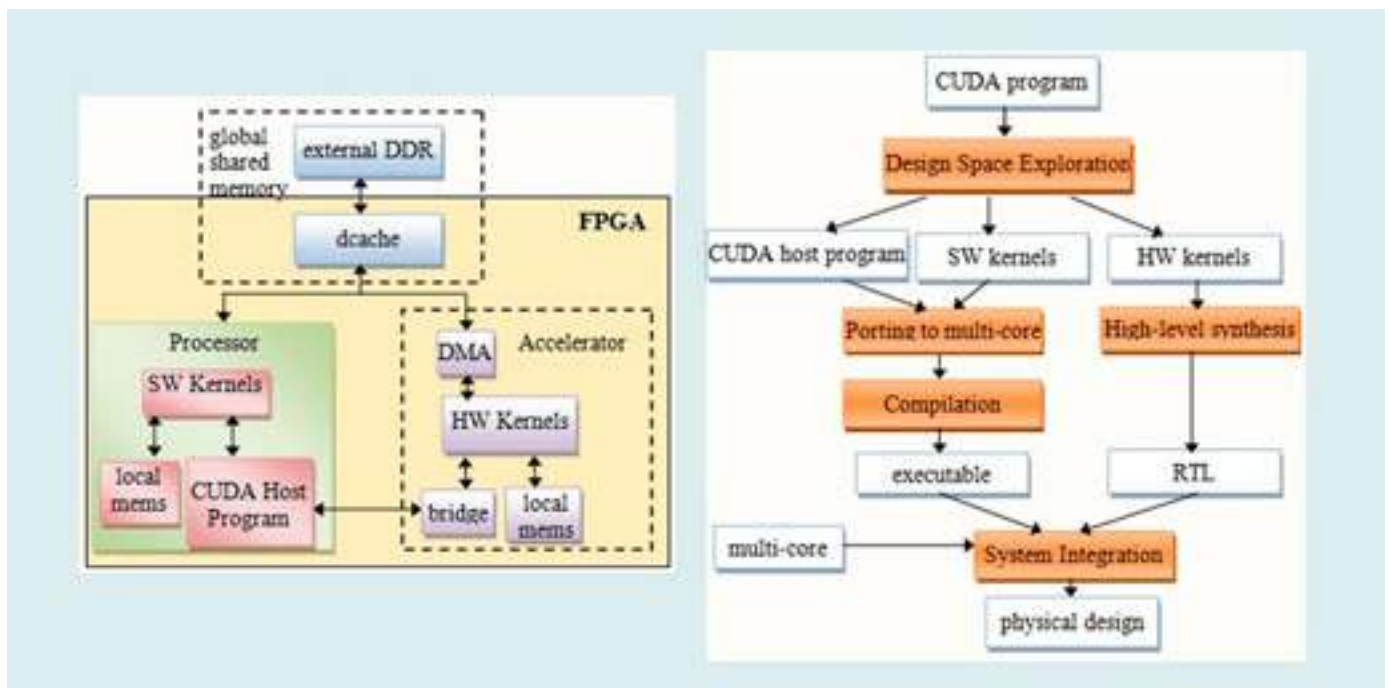
Several scientific applications such as graphics, biological modeling, molecular dynamics, fluid dynamics, environmental simulations and others, usually involve many independent iterations of the same piece of code. Such iterations can be efficiently executed by parallel architectures, such as multi-core processors, Graphical Processing Unit (GPUs) and FPGAs. GPUs have been traditionally favored over multi-core processors for running such applications. In the same way, FPGAs can potentially provide even higher speedups at lower power consumption than GPUs. Low-power FPGAs provide the processing power and logic capacity to implement and efficiently execute several parallel portions of an application. Their use is, however, still limited, since the path to porting an application onto FPGA custom hardware is often prohibitively cumbersome.

FASTCUDA has managed to facilitate this path by providing a novel methodology, architecture and toolset to automatically port and run already-parallelized algorithms on reconfigurable hardware. For this purpose, the FASTCUDA methodology proposes the use of CUDA, a Graphical Processing Unit (GPU) language, which exposes parallelism at the source level. FASTCUDA provides a design methodology and accompanying toolset that allows CUDA programs to be executed efficiently on a shared memory, multi-core processor communicating with an FPGA-based accelerator. Using FASTCUDA, compute-intensive parallel portions of an application can be automatically synthesized and implemented with multiple special-purpose accelerators in hardware. The figure shows the block diagram of the overall system

architecture, as well as the tool flow. The FASTCUDA toolset first splits the CUDA kernels into two parts: one part will be compiled and executed as parallel software on an embedded multi-core processor, and the other part will be synthesized and implemented with multiple special-purpose accelerators in hardware. The multi-core processor is used to run the CUDA host program serially and execute the software CUDA kernels in parallel. Threads belonging to the same CUDA thread-block are executed by the same core. The hardware CUDA kernels are partitioned into thread-blocks, and synthesized and implemented inside an “Accelerator” block. Each software or hardware thread-block has a local private memory, while the global shared memory can be accessed by any thread, following the philosophy of the CUDA model. The FASTCUDA toolset is responsible for automating most of this process, thus minimizing user intervention, and consequently, increasing design productivity [1]. Some first evaluation results have shown that hardware execution of a compute-intensive CUDA kernel is about ten times faster than software execution.

[1] An initial version of the toolset can be downloaded from the following link: <http://sourceforge.net/projects/fastcuda/>

Iakovos Mavroidis, Luciano Lavagno, Ioannis Papaefstathiou, (Mavroidis, Papaefstathiou: Microprocessor and Hardware Lab, Technical University of Crete, Greece), (Lavagno: Department of Electronics, Politecnico di Torino, Italy)



FP7 TRANSFORM PROJECT - THEORETICAL FOUNDATIONS OF TRANSACTIONAL MEMORY

The research project TransForm, coordinated by the Institute of Computer Science of the Foundation for Research and Technology – Hellas (FORTH), has recently been completed.

TransForm: Theoretical Foundations of Transactional Memory. The research project TransForm, coordinated by the Institute of Computer Science of the Foundation for Research and Technology – Hellas (FORTH), has recently been completed. TransForm was a project funded by the European Commission in the context of the Marie Curie Initial Training Network Action. The project contributed significantly to building the theoretical underpinnings for the design and analysis of Transactional Memory (TM) systems.

The widespread adoption of multi-core processors has led to a new software revolution, the concurrency revolution. Despite the fact that concurrency is almost as old as computing and a large number of concurrent programming models and languages have been proposed in the past, reducing the difficulty of parallel programming is still a necessity. So, the revolution is about much more than concurrency alone: it is about concurrency for the masses.

Transactional Memory is a new programming paradigm which is considered promising by many researchers, and which has led to a plethora of publications in the past ten years. A deep understanding of the capabilities and properties of TM systems is highly desirable, in order to better understand such systems, as well as allowing thorough evaluation and the means to greatly improve them. Project TransForm significantly contributed in this direction. It explored the semantics of TM systems and formulated a common framework for the design of TM algorithms and comparison of their performance.

As a result of the research efforts of the project, correctness and progress criteria for such systems were proposed and suitable complexity metrics were intro-

duced. Moreover, efficient implementations of TM systems were designed and tested, and fundamental software structures such as shared data structures were efficiently implemented on top of them. Finally, some of the inherent limitations of such systems were discovered; these limitations must be taken into account when designing TM systems.

TransForm offered high-quality education to twelve Early Stage Researchers (ESR) who were employed for the needs of the project. Those researchers were at an early stage of their research career, being in possession of a Masters (MSc) degree and not a Doctoral (PhD) title. Through their participation in the network, they were offered appropriately structured training in the research area of the project, namely concurrent computing. They were also exposed to additional training activities, which armed them with the required complementary skills for a successful career. Last but not least, the project brought the ESRs in contact with other professional environments such as industry. Most of the ESRs participated in the graduate studies programmes of the organizations they worked for (or the universities co-located with these organizations), for the purpose of obtaining a PhD, and have been adequately trained through the work in the project for this purpose. Project TransForm conducted research that can contribute to the following areas in the future.

The research results conducted in TransForm are already seen as a point of reference for the design and analysis of concurrent algorithms, be they TM-oriented or not. Moreover, the research efforts of the project shed light on fundamental issues of the design and analysis of TM systems and contributed to the accurate comprehension of their actual properties. This can

facilitate the widespread adaptation of those systems and consequently the easier production of concurrent software.

Finally, TransForm has led to the creation of a powerful network of collaboration between academic and research organizations and industry, which aims at efficiently using parallelism in order to fully exploit the available computational power that multi-core processors have or will have to offer in the future. TransForm lasted for three years. Five organizations participated, with Greece being the project coordinator through the Foundation of Research and Technology Hellas (FORTH). The other organizations were the Swiss Federal Institute of Technology in Lausanne (École Polytechnique Fédérale de Lausanne – EPFL) in Switzerland, the Berlin University of Technology (Technische Universität Berlin – TUB) in Germany, the Technion – Israel Institute of Technology, and the University of Rennes 1 (Université de Rennes 1) in France. The project was further supported and co-supervised by a board of industrial partners: Deutsche Telekom (Germany), Microsoft Research (Cambridge, United Kingdom), Oracle Labs (Massachusetts, USA), IBM (T.J. Watson Research Center, USA). Contact Information Dr. Panagiota Fatourou, Assistant Professor Foundation for Research and Technology – Hellas (FORTH) Institute of Computer Science (ICS) N. Plastira 100, Vassilika Vouton GR-70013 Heraklion, Crete, Greece Tel. +30 2810391727 Fax +30 2810391609 Email: faturu@ics.forth.gr

Dr. Panagiota Fatourou, Assistant Professor, Foundation For Research and Technology – Hellas, Institute of Computer Science

FP7 PHARAON PROJECT

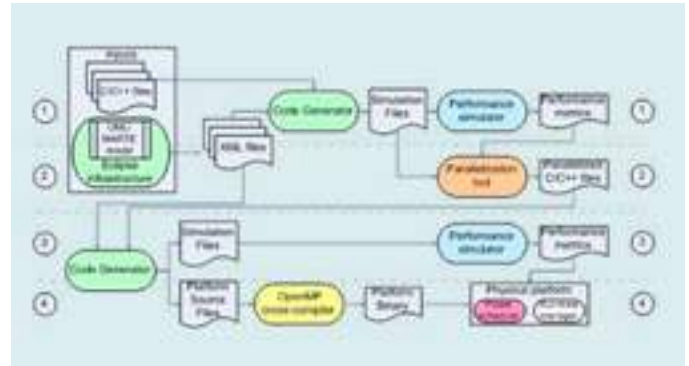
Improving the design flow for parallel and heterogeneous architectures running real-time applications

Recent market analyses show that there is an important increase in the number of multicore architectures used in projects. During the last decade, those architectures have expanded from only targeting some very specific domains with very high processing needs (e.g. engine control), to become the actual implementation paradigm for mainstream embedded systems. This kind of architectures is getting increasing acceptance into the computing industry, and has become very common for the mass market electronic devices segments (e.g., smartphones, tablets, internet boxes, etc...). Now, even for harsh environment markets having safety, security and hard real-time constraints, multicore architectures are becoming unavoidable.

Designers are facing challenging problems as hardware architectures are evolving faster than multicore software development techniques. And applications in need of this extra computing power are evolving even faster. These techniques are not yet capable to provide efficient methodologies to exploit the full potential of multicore architectures satisfying all the requirements of embedded systems, including performance and power consumption. Accurately predicting the performance of an application implemented on such architectures has become very difficult, because of numerous factors such as cache coherency. Moreover, commonly taught programming models, that are generally based on sequential languages, are no longer sufficient, since early consideration of parallelism in applications has become critical. The lack of efficient software design techniques increases both software development costs and implementation risk in terms of costs and delays. Parallelism, heterogeneity, complex memory structures, efficient power monitors and controllers, are among the list of new functionalities provided by recent multicore systems that require to be adequately tackled by new design tools, as proposed by the **PHARAON project** which will end by August 2014 after three years of work and collaborations.

The objective of European collaborative project FP7 288307 PHARAON partially funded by the European Commission is to achieve a breakthrough towards broader adoption of multicore architectures and to enable the development of complex systems with high processing needs and low-power requirements. For such purpose, the project focuses on solving two major problems appearing in these types of systems and the reduction of power consumption to benefit for longer autonomy. **The targets of the project are to reduce the software development cost by 25% and to increase the battery life of embedded systems by nearly 20%.**

To reach this objective, the project has developed two different sets of techniques and tools. The first set directly affects the design flow, from UML/MARTE specifications to implementation on multicore platforms. The objective is to assist the designer in finding the most adequate software architecture while taking into account hardware constraints at design time. To do so, tools



developed in PHARAON can evaluate the parallel structure of an application and propose improvements, in terms of parallelization constructs. At the same time, the toolset will be able of automatically generating the multi-processor embedded code required to deploy the communicating SW components on the processing cores of the system, including DSPs and GP-GPUs.

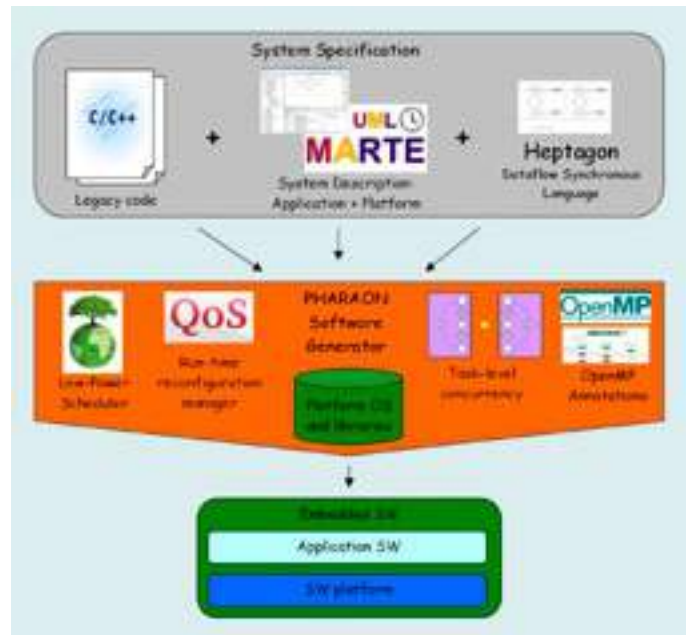
The second set of techniques and tools affect the runtime behavior of the application. The objective is to adapt the performance of the platform (frequency and voltage, for example) in order to consume only the required energy. For this purpose, project partners are developing monitoring and control techniques that are integrated in the code generated at design time to map the SW to the processors of the platform. This middleware automatically adapts platform services to application requirements during execution, and therefore reduces power consumption.

The PHARAON approach and tools have been successfully evaluated on two industrial application domains (radio and stereovision). The main target platforms for experimentations have been the intel i5 3570T and the Freescale i.MX6Q-SDP (Quad ARM A9 + Vivante GPGPU). In terms of quantitative results, software development time has been reduced thanks to the code generation approach and thanks to the parallelization toolset that have enabled **speed-up of x4 times** on the two use cases on the quad core architectures compared to the baseline sequential code. Concerning power saving, the tools developed have enabled **processor power reduction of 20%** by offering the same level of performance. The outcomes of the project have been presented at several respected conferences (**DAC, DATE**) and journal papers (**ACM, IEEE**). **Patents** have also been filed during the project time frame.

The overall approach and the tools developed during the project are described below (more information is also available on the project website):

IMPROVEMENT ON THE SOFTWARE DESIGN FLOW PART CONTRIBUTED BY TOOLS THAT CAN BE CONNECTED TOGETHER:

- *UML/MARTE modeling combined with code generation* (<http://www.essyn.com>) The PHARAON design flow starts with the well-known component based approach to design the applications. The approach is software centric, and assumes an allocation of components to programmable processors. At this stage a first coarse-grained parallelization can be done. The main achievements that allows to reduce development time have been in the generation of code for the following: Code generation supporting heterogeneous architectures (GPP-DSP and GPP-GP-GPU), Code generation supporting I/Os calls, code generation supporting fine grained parallelisation (OpenMP/OpenCL), and code generation enabling inputs for the other tools in the PHARAON toolchain
- *Performance and energy estimator from the commercial parallelization toolchain Pareon* (<http://www.vectorfabrics.com/products>). Pareon contains tools for estimating timing and energy consumption of C/C++ applications. The estimates are fed into the ParTools to help parallelize performance and optimize memory bottlenecks of the code, while tracking effects on power consumption. Furthermore, the energy estimates are used by the low power scheduler that can select the most power-efficient operating mode of the system.
- *ParTools parallelisation toolset* (<http://sourceforge.net/projects/partools/>) This tool addresses the parallelization of legacy sequential C software that can include also complex control structures, pointer operations, and dynamic memory allocation. The views offered by the tool can substantially speed up the parallelization decisions made by the developers by tracking data dependencies through variables inside any scope or storage class, including those that are dynamically allocated on the heap.
- *OpenMP extension for data-flow and stream parallelism* (<http://www.openstream.info/>). OpenStream is a stream programming language, designed as an incremental extension to the OpenMP programming language, which allows expressing arbitrary task-level data flow dependence patterns. Programmers expose task parallelism and provide data-flow information to the compiler through compiler annotations (pragmas), used to generate code that dynamically builds a streaming program. The language supports nested task creation, modular composition, variable and unbounded sets of producers/consumers, and first-class streams. These features, enabled by an original GCC-based compilation flow, allow translating high-level parallel programming patterns into efficient data-flow code



REDUCTION OF POWER CONSUMPTION THROUGH MONITORING AND DVFS/DPM DECISIONS TAKEN AT RUNTIME:

During the application run, due to the scalable resources available by multicore architectures and the scalability of running applications (QoS), various opportunities can be exploited by a Middleware to optimize application and hardware platform performance. Such run-time decisions are organized into two layers:

- A *Global runtime Manager* (proprietary tool) that takes care of coarse grained level which includes decisions triggered periodically or by dynamic events (low level battery signal, change in the user QoS, new application registered, etc..). This module includes the optimal selection of the application configuration (Pareto set defined at Design time) and then the (re)mapping on the platform resources.
- A *Low-Power scheduler* (proprietary tool) that takes care of fine grained decisions to improve application performance by monitoring slack time in the application. It takes as an input the selected application configuration mode defined the Global runtime manager. By monitoring application timing and comparing them with the Worst Case Execution Time (WCET), DVFS decisions are taken during tasks execution to provide the lowest performance/power mode while still complying with the application real-time constraints.

<http://pharaon.di.ens.fr/>

Thales Communications & Security, France; Tedesys, Spain; Vector Fabrics, Netherlands; IMEC Leuven, Belgium; Ecole Normale Supérieure-INRIA, France; Politecnico di Torino, Italy; University of Cantabria, Spain

FP7 RETHINK BIG PROJECT: ROADMAP FOR EUROPEAN TECHNOLOGIES IN HARDWARE AND NETWORKING FOR BIG DATA

Project name: RETHINK big: Roadmap for European Technologies in Hardware and Networking for Big Data
Coordinator: Dr. Adrián Cristal and Gina Alioto, Barcelona Supercomputing Center – Centro Nacional de Supercomputación (BSC-CNS)
Partners: BSC-CNS, Spain
 TUB, Germany
 EPFL, Switzerland
 CWI, Netherlands
 UniMan, United Kingdom
 UPM, Spain
 ARM, United Kingdom
 ParStream, Germany
 IMR, France
 No Rack, France
 Thales, France
 ALBLF, France
Start date: March 2014
Duration: 24 months
Website: www.rethinkbig-project.eu

Big Data is so much more than Hadoop, MapReduce, High Performance Computing and Data Centers. There is a completely new world of not-yet-even-dreamed-of systems and applications that is waiting to be discovered. But, in order to discover this world, we not only need to utilize new software and tools, but also the novel hardware and networks that will allow us to have the computational power, the storage capacity, the communication bandwidth and the power envelope that the next era in Big Data is already demanding. Today, Big Data is in its infancy, and Europe is in the best possible position to lead the Big Data revolution. Europe is home to the most power-efficient chip designs, we are world leaders in embedded computing, and we have extensive expertise in sensors. We also lead in many of the emerging software domains for Big Data: healthcare, smart cities, and the Internet of Things. Europe's biggest challenge today is to integrate these assets in a vertical way to tap into our full potential. The RETHINK big Project is here to create a roadmap that allows Europe to combine its strength in hardware and software to become the world reference in Big Data.

The objective of the RETHINK big Project is to bring together the key European hardware, networking, and system architects with the key producers and consumers of Big Data to identify the industry coordination points that will maximize European competitiveness in the processing and analysis of Big Data over the next 10 years. Specifically, RETHINK big will deliver a strategic roadmap for how technology advancements in hardware and networking can be exploited for the purpose of data analytics and beyond while also taking into consideration advancements in applications, algorithms and systems.

Practically speaking, the roadmap will be produced as a result of area specific and cross-functional working group meetings and congresses. The project is currently evaluating the existing competencies across European Big Data application domains and technology providers in Europe as well as identifying the key European stakeholders, or the established and up-and-coming institutions that possess or are developing the technologies, processes or services that map to these competencies. From these stakeholder institutions, we are selecting technology and business experts that will chart the technological advancements, their respec-

tive challenges and the potential business opportunities that they present.

The RETHINK big Project is a two-year project funded by the European Union's Seventh Framework Programme with a budget of over 1.9M€. The project started on March 1, 2014 and was kicked-off in a series of co-located meetings with European Data Forum 2014.

Coordinated by the Barcelona Supercomputing Center (Spain), the RETHINK big Project brings together leading European organizations in Big Data and Hardware and Networking technologies including Technische Universität Berlin (Germany), Centrum Wiskunde & Informatica (Netherlands), École polytechnique fédérale de Lausanne (Switzerland), The University of Manchester (UK), Universidad Politécnica de Madrid (Spain), ARM Limited (UK), ParStream GmbH (Germany), Internet Memory Research SAS (France), No Rack SAS (France), Thales (France) and Alcatel-Lucent Bell Labs (France)

Dr. Adrián Cristal and Gina Alioto, Barcelona Supercomputing Center – Centro Nacional de Supercomputación (BSC-CNS)



COLLABORATION GRANT REPORT - MICHEL STEUWER



Performance-portable parallel patterns for heterogeneous system

Computing systems have become increasingly complex and difficult to program with the emergence of heterogeneous hardware. For instance, it is now common to see GPUs (Graphic Processing Units) used for general purpose computation in personal computers, data centres or even supercomputers. As a result, achieving high performance and energy-efficiency for such complex systems is an extremely challenging task.

High-level programming languages have been proposed to address this issue. However, they often rely on complex analysis in the compiler and device-specific implementations to achieve maximum performance. As a result, compilers and software implementations need to be re-tuned for every device.

In our collaboration we started to design and implement a system offering performance portability in a systematic way. For a four month period I was visiting Christophe Dubach from the Institute for Computer Systems Architecture (ICSA) at

the University of Edinburgh. We closely collaborated in designing a high-level programming system based on algorithmic patterns which programmers use to describe their application. The high level algorithmic patterns are systematically transformed into a lower-level form which is amenable to high-performance OpenCL code generation. We use a set of powerful, yet simple, transformation rules for this process. As all rules preserve the original semantics of the program we can safely use automatic search techniques to explore different optimizations by systematically transforming the code. By design the code generation process is straightforward, since all optimization decisions are made as part of the search process. During the collaboration we developed a prototype implementation which already generates code matching the performance of highly tuned OpenCL implementations. Among other benchmarks we evaluated the level 1&2 BLAS routines on CPUs and GPUs by AMD, Intel, and NVIDIA. Our prototype generates code matching the performance of CUBLAS on Nvidia GPUs,

MKL on Intel CPUs, and even outperforms by up to 4.5 times on an AMD GPU their own clBLAS implementation.

The HiPEAC collaboration grant is a great opportunity for PhD students like me to experience international research, meet interesting people, and see different perspectives on specific problems as well as on research in general. The collaboration allowed us to combine the strength of our different backgrounds and experiences to design a powerful novel system in a short period of time. I'm very grateful to the HiPEAC network for funding the collaboration. I would also like to thank my supervisor Sergei Gorlatch for his support and flexibility, which made this collaboration possible, as well as my host Christophe Dubach and everybody at ICSA in Edinburgh who made me really feel welcome.

*Michel Steuwer,
University of Muenster, Germany*

COLLABORATION GRANT REPORT - DAVIDE ZONI



I have a post-doc position at the Politecnico di Milano - Dipartimento di Elettronica, Informazione e Bioingegneria (DEIB). My research activities are mainly focused on power-reliability-performance optimization in Networks-on-Chip, considering hardware design aspects as well as the exploitation of control theory. Thanks to the HiPEAC grant I had the opportunity to spend four months during summer 2013 at the Universitat Politècnica de València (GAP research group) working with Prof José Flich.

The internship focused on the power-performance exploration and optimization of Networks-on-Chip (NoCs). Such interconnection fabric is considered a promising, efficient, reliable and flexible communication infrastructure for multi-core platforms.

To this purpose, suitable power-performance methodologies have to be designed, since the power consumption is not negligible and the overall chip performance is strongly influenced by this communication layer.

In this perspective, the research has been split in two main sections. First, we focused on the combination of different techniques to aggressively optimize power and performance, in contrast to other proposals addressing the power/performance optimization in NoCs, which consider a single technique at a time. In particular, Dynamic Voltage and Frequency Scaling (DVFS) and Multiple Static Frequency Island (MSFI) solutions have been considered in combination with different routing algorithms, namely deterministic XY routing as a baseline and

adaptive routing schemes based on Duato's routing theory. Second, power and performance overheads of the DVFS actuator have been investigated to take into account the impact they have on the benefits obtained by each evaluated methodology.

Power and timing estimates have been collected from both simplified PLL and Voltage Regulator models described in SPICE. Starting from these estimates we characterized a two-pole transfer function that has been integrated in the simulation environment used for the experiments to account for the timing overheads due to dynamic voltage and frequency adjustments. Moreover, the worst-case DVFS

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power consumption is used to represent the power overhead.

At the end of the research, a complete analysis has been done of the integration of different orthogonal strategies to balance power and performance in the NoC, as well as making a suitable set of tools available and integrated for further analysis.

I would like express my appreciation to the HiPEAC NoE for this excellent opportunity, which allowed me to establish a cooperation bridge with a different European research group, with a mutually profitable sharing of competencies, a valuable meeting of interesting people and the creation of a long-term scientific contact between two universities. In particular, I would like to thank Prof José

Flich for his guidance and the rest of the people composing his research group who allowed me to feel at home during my stay. I think all PhD students and young researchers may greatly benefit from the collaboration grants sponsored by HiPEAC

Davide Zoni, Politecnico di Milano

COLLABORATION GRANT REPORT - HADI SADEGHI TAHERI

I am a PhD student at Ghent University, working on contemporary compilation techniques for code optimization for many core accelerators (specifically Coarse Grain Reconfigurable Arrays or CGRAs). The focus of my research includes optimizing and parallelizing loops in Static Single Assignment (SSA) Intermediate Representation (IR), based on LLVM, an open source, standard and state of the art compiler.

As part of a HiPEAC-sponsored industrial internship, I spent four months at Movidius in Dublin, Ireland. Movidius designs compact, high performance, ultra low power vision processor chips that enable computational imaging and visual awareness. Currently Movidius' products are being used in Google's intelligent devices, as well as some other mobile platforms. While much of my own work focuses on IR-level optimization, I intended to learn more about the compiler's back-end.

Thanks to HiPEAC and Movidius, I had the chance to work on an Industrial LLVM back-end with a group of expert engineers. During the period of internship, we were working on SHAVE's back-end to improve its compatibility with the most recent version of LLVM and to increase its performance as well. SHAVE is an ultra low-power VLIW-like co-processor with the capability of running in DSP and SIMD modes. I had the chance to become more familiar with back-end design methods and issues and participate in the SHAVE back-end implementation, specifically using LLVM's TableGen methodology. TableGen provides a high-level object-oriented description of the processor's ISA and register file, which is specifically designed to allow the writing of flexible descriptions, factoring out common features of these records. This reduces the amount of duplication in the description, reduces the chance of error, and makes it

easier to structure domain-specific information. In addition to working on the back-end, I was able to work on LLVM's Loop Unroll pass and modify it to generate fewer branch instructions through Loop Unrolling, so there is more opportunity for Instruction Level Parallelism (ILP) inside unrolled loops.

I would like to express my gratitude to HiPEAC for providing this excellent opportunity. It allowed me to see the connection between research and industry, meet interesting people and establish long term contacts. I am also grateful to Movidius for hosting me.

*Hadi Sadeghi Taheri
Ghent University, Belgium*



A THREE-DIMENSIONAL REPRESENTATION METHOD FOR NOISY POINT CLOUDS BASED ON GROWING SELF-ORGANIZING MAPS ACCELERATED ON GPUS



Sergio Orts-Escolano, University of Alicante, Spain
Advisor: Jose Garcia-Rodriguez and Miguel Cazorla Quevedo
Graduation date: January, 2014

The research described in this thesis was motivated by the need for a robust and efficient model capable of representing 3D data obtained using 3D sensors, which are inherently noisy. In addition, time constraints were considered, since these sensors are capable of providing a 3D data in real time. This thesis proposed the acceleration of Self-Organizing Maps for 3D data representation. It was proposed to parallelize and optimize the Growing Neural Gas algorithm, leveraging the computing power of modern GPUs. The method was applied to different problems

and applications in the area of computer vision, such as the recognition and localization of objects, or 3D scene reconstruction. Moreover, research was conducted on the integration of 3D data processing algorithms into complex computer vision problems. Experiments demonstrated that the GPGPU paradigm allows 3D data processing to be considerably accelerated, compared with CPU implementations, allowing real-time execution.

SOFTWARE-DEFINED RADIO: CHALLENGES AND OPPORTUNITIES IN BASEBAND PROCESSING ARCHITECTURES

Omer Anjum, Tampere University of Technology, Finland
Advisor: Jari Nurmi
Graduation date: March 2014

In the initial phase of this work an MPSoC based on a general purpose RISC Processing Engine was considered, where the gain after splitting the application over multiple cores was a 6.1x speed up compared with a single PE. However, using a RISC processor to execute DSP tasks is not the best tradeoff point among speed, area and power consumption, needed for an SDR platform. Several experiments were then

made to explore DSP, conventional ASIP and Transport Triggered Architecture (TTA), with LTE and WLAN as test cases. TTA gave a promising trade-off among speed, area and power consumption. In one of the test cases a single TTA core was even 1.9 times faster than an MPSoC consisting of nine RISC cores. TTA has also been proven as more energy efficient when compared to other more optimal architectures. However, the instruction memory for TTA grows exponentially through the increase in the number of buses. A conventional ASIP with task-level instructions for time-consuming DSP operations, such as FFTs, gives a performance closer to an ASIC and

helped to reduce the instruction memory significantly, at the cost of flexibility. Whether we need more flexibility is left as an open question to the reader. At the algorithmic level of exploration, an efficient realization of a finite-impulse response (FIR) filter bank consisting of L filters with equal pass-band bandwidths was constructed with few additional multipliers and adders, which are needed to design the prototype filter. It was also possible to perfectly reconstruct the signal with just a single adder.

PERFORMANCE ASPECTS OF SYNTHESIZABLE COMPUTING SYSTEMS

Pascal Schleuniger, Technical University of Denmark
Advisor: Dr. Sven Karlsson
Graduation date: April, 2014.

This thesis addresses performance aspects of synthesizable computing systems on FPGAs. It evaluates how a processor architecture can exploit current state-of-the-art FPGA structures. An exposed

processor pipeline is proposed to enable a fast system clock and to keep the hardware resource usage low. It is investigated whether a compiler, GCC, is able to generate efficient code for the proposed architecture. The evaluation of the implemented processor pipeline shows that the proposed approach enables an average performance improvement of 56% and requires 35% fewer hardware resources than commercial processor

cores. Moreover, this thesis describes the design of communication structures for multicore configurations, evaluates the scalability of these systems, and discusses how to efficiently program them.



UNDERSTANDING MULTICORE PERFORMANCE: EFFICIENT MEMORY SYSTEM MODELING AND SIMULATION



Andreas Sandberg, Uppsala University, Sweden
 Advisor: Prof. Erik Hagersten & Dr. David Black-Schaffer
 Graduation date: May, 2014

Efficient models are essential when trying to understand the performance of a computer system. I have demonstrated three efficient modeling strategies that do not incur the overhead of traditional simulation. First, I show how a sampled memory access profile can be used to drive automatic cache optimizations and to qualitatively classify an application's last-level cache behavior. Second, I demonstrate

an efficient quantitative model for shared last-level caches, which provides insights into how data locality affects sharing. Third, in order to model future systems, I demonstrate an efficient sampling simulator that leverages hardware virtualization to accelerate sampling.

HIERARCHICAL TRANSPARENT PROGRAMMING FOR HETEROGENEOUS COMPUTING



Yuri Torres de la Sierra, Universidad de Valladolid
 Advisor: Arturo González Escribano and Diego R. Llanos Ferraris
 Graduation date: May, 2014

In my Ph.D. thesis, we study the possibility of developing a portable and transparent programming system that incorporates hierarchical tiling and scheduling policies in order to take advantage of heterogeneous environments. To accomplish our research proposal, we take advantage of the Hitmap library. Hitmap is a prototype framework that integrates a parallel computation model capable of exploiting all available hardware resources (CPU and GPU) in a heterogeneous system. We present a study of GPU architectures to help to determine good values of the configu-

ration parameters that should be chosen by the programmer. The knowledge obtained from this study is used to create proper policies for selecting the configuration parameter values for the GPU. After analyzing these results, we consider whether a programming execution is feasible containing automatic data partitioning techniques, communication tools, and the transparent selection of good values of the GPU configuration parameters.

PERFORMANCE-AWARE COMPONENT COMPOSITION FOR GPU-BASED SYSTEMS



Usman Dastgeer, Linköping University, Sweden
 Advisor: Prof. Dr. Christoph Kessler
 Graduation date: May 2014

This thesis investigates the design and implementation of frameworks for component-based programming of GPU-based systems. Program components representing a specific functionality can encapsulate multiple implementations of that computation on the same or different types of execution units, such as CPU cores or GPUs. Automated implementation selection and memory management mechanisms lead to better programmability, portability and performance. The

thesis work makes key contributions to the design and implementation of three different approaches and prototype frameworks: the SkePU tuneable skeleton programming library, the PEPHER component model and composition framework, and the Global Composition Framework.

PERFORMANCE ANALYSIS METHODS FOR UNDERSTANDING SCALING BOTTLENECKS IN MULTI-THREADED APPLICATIONS



Kristof Du Bois, Ghent University, Belgium

Advisors: Prof. Dr. Lieven Eeckhout, Dr. Stijn Eyerman

Graduation date: June, 2014.

In this dissertation, we propose new methods for analyzing multi-threaded applications and identifying scaling bottlenecks. Our first method, called criticality stacks, is useful for understanding parallel (im)balance between threads. The second method, bottle graphs, visualizes parallel performance bottlenecks by quantifying both execution time and parallelism for each thread. Finally, we present speedup stacks, which is a tool for providing insights

into an application's scaling behavior on multi-core hardware. We illustrate the usefulness of these three methods for analyzing parallel performance, as well as for guiding software source code optimization, dynamically optimizing performance, and reducing energy consumption of parallel programs.

SPEEDING UP ARCHITECTURAL SIMULATION THROUGH HIGH-LEVEL CORE ABSTRACTIONS AND SAMPLING



Trevor E. Carlson, Ghent University, Belgium

Advisor: Prof. Dr. Lieven Eeckhout

Graduation date: June 2014

Single-threaded microarchitecture simulators are unable to take advantage of modern multi-core systems. The simulation gap widens, as simulators cannot keep pace with processor performance. My Ph.D. research describes solutions for hardware-software optimization. For this purpose, we developed Sniper, a fast and accurate microarchitectural open-source simulator. In addition, we propose a new core model, the Instruction-Window Centric model, allowing for higher accuracy with almost the same simulation speed as high-

level core models. Sniper 6.0, released in June 2014, now ships with this core model. You can find it at <http://snipersim.org>. Additionally, we detail the first general-purpose multi-threaded sampling technique, and its extension to barrier-based applications, BarrierPoint, which significantly reduces detailed application simulation. With BarrierPoint, we show maximum speedups of up to 800 times.

UPCOMING EVENTS

THE 10TH INTERNATIONAL CONFERENCE ON WIRELESS AND MOBILE COMMUNICATIONS (ICWMC 2014)

July 22-26, 2014, Seville, Spain

<http://www.iaria.org/conferences2014/CfPICWMC14.html>

THE 20TH INTERNATIONAL EUROPEAN CONFERENCE ON PARALLEL AND DISTRIBUTED COMPUTING (EURO-PAR 2014)

August 25-29, 2014, Porto, Portugal

<http://europar2014.dcc.fc.up.pt/>

THE 24TH INTERNATIONAL CONFERENCE ON FIELD PROGRAMMABLE LOGIC AND APPLICATIONS (FPL 2014)

September 2-4, 2014, Munich, Germany

<http://www.fpl2014.org/>

24TH INTERNATIONAL WORKSHOP ON POWER AND TIMING MODELING, OPTIMIZATION AND SIMULATION (PATMOS 2014)

September 29-30, 2014, Palma de Mallorca, Spain

<http://www.uibcongres.org/patmos-variz2014/>

1ST WORKSHOP ON METHODS AND TOOLS FOR DATAFLOW PROGRAMMING (METODO)

Colocated with DASIP 2014 - Madrid, Spain Tuesday, 7 October 2014

<http://www.ecsi.org/dasip/metodo2014>

INTERNATIONAL SYMPOSIUM ON SYSTEM-ON-CHIP, SoC 2014

Tampere, Finland, October 28-29, 2014

<http://soc.cs.tut.fi/2014/index.php>

THE NORDIC MICROELECTRONICS CONFERENCE NORCHIP 2014

Tampere, Finland, October 27-28, 2014.

<http://www.norchip.org/>

THE 47TH INTERNATIONAL SYMPOSIUM ON MICROARCHITECTURE (MICRO-47)

December 13-17, 2014, Cambridge, UK

<http://www.microarch.org/micro47/>

THE 10TH INTERNATIONAL CONFERENCE ON HIGH PERFORMANCE AND EMBEDDED ARCHITECTURES AND COMPILERS (HIPEAC 2015)

January 19-21, 2015, Amsterdam, The Netherlands

<http://www.hipeac.net/conference>

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