Information Society Technologies

HiPEAC info 2

COMPILATION ARCHITECTURE

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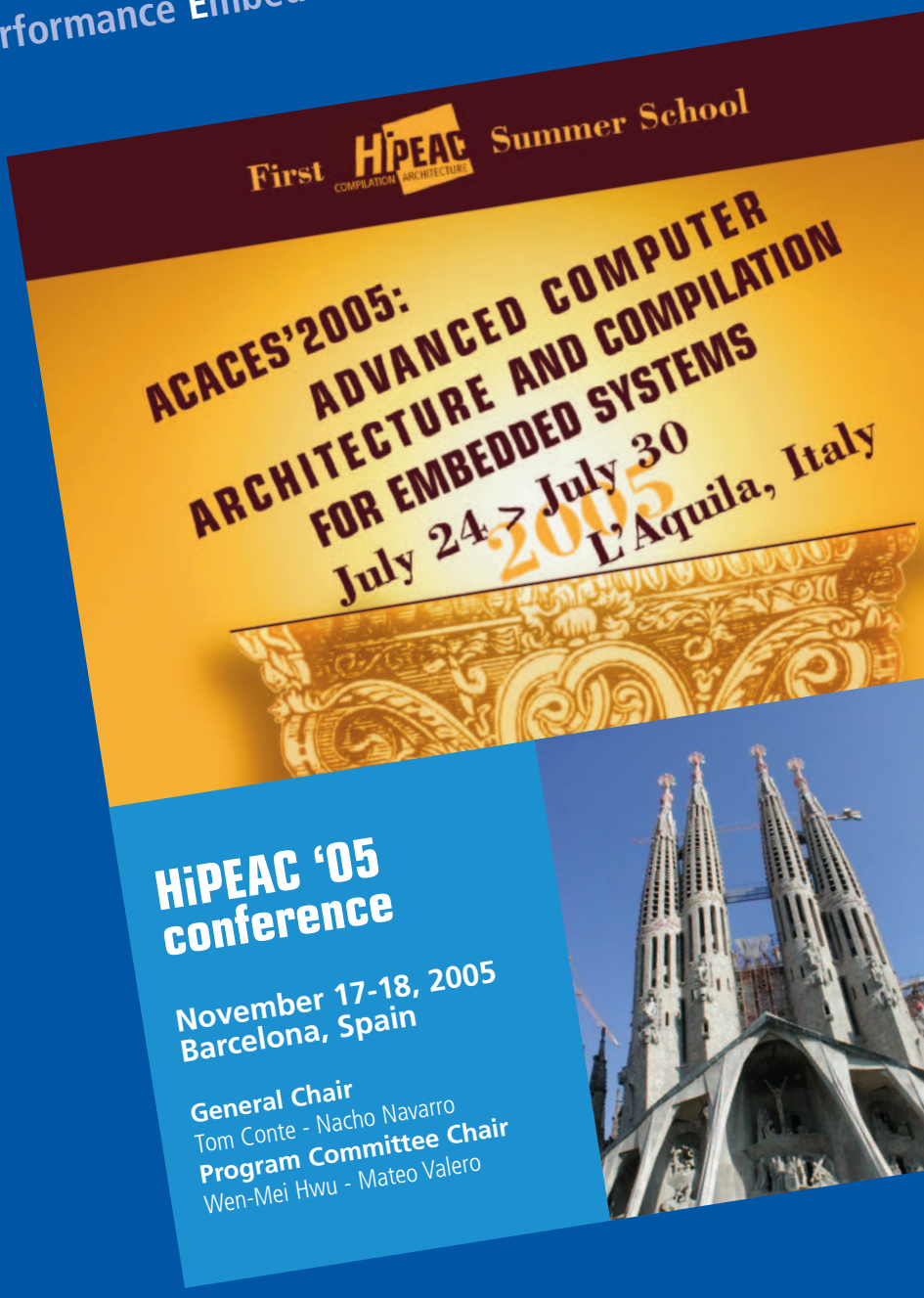
Network of Excellence on High Performance Embedded Architectures and Compilers



www.hipeac.net

Call 5 of the IST priority Strategic objective 'Embedded Systems'
Deadline: 21 September 2005
www.cordis.lu/ist/so/embedded-systems/home.html

Message from the HiPEAC coordinator

Mateo Valero
Coordinator
UPC Barcelona
mateo@ac.upc.edu

Dear colleagues,
I am glad to have the opportunity to share with you my view on the results that HiPEAC has achieved so far and what our next steps should be. During the last few months we have been working hard in order to offer to our community two high quality events that will take place during 2005: the HiPEAC Summer School (July 05), with the participation of top lecturers, including several Eckert-Mauchly award winners; and the HiPEAC Conference in Barcelona (November 05), with a world-class Steering and Program Committee. Those should be very good chances to meet and work together, so you may want to make space in your agenda already!

HiPEAC has also completed its first call for collaborations, with more than € 180 000 distributed amongst 25 HiPEAC members for collaboration purposes.

All HiPEAC members are entitled to participate in these calls, so stay tuned for more very soon. We aim to have dynamic processes with low administrative burden, which means a very straightforward application form for you! Our new website will keep you updated.

The HiPEAC community continues to work closely with the European Commission RTD Framework Programmes. Within FP6, several proposals will be submitted under the Future and Emergent Technologies call for Advanced Computer Architectures and under the IST call for Embedded Systems. We aim to maintain a close collaboration with the EC during the future FP7, continuing the HiPEAC tradition of excellence.

In our first newsletter we stated that the core HiPEAC mission was to act as a steering partner for researchers. Certainly, our ambitious scientific and organizational goals defined then cannot be accomplished without your participation. My wish as HiPEAC coordinator would be therefore to see that all our efforts combine to build a stronger, more vibrant community. Ultimately, the results achieved by HiPEAC's participants will be the measure of HiPEAC's own success. ■

Message from the project officer

On 17th May 2005 we anticipate the publication of the 5th IST call for proposals based on the Work Programme for 2005 and 2006. I would like to draw the attention of the HiPEAC community to the Strategic Objective on Embedded Systems. We will be calling for proposals on design methods, programming models and compilation tools for reconfigurable architectures.

This research complements the Strategic Objective on Nanoelectronics; the latter focuses on chip design including SoC and SiP, whereas in Embedded Systems the focus is on system design, from the application down to the embedded platform architecture.

We expect to receive both STREPs and Integrated Projects. STREPs are intended to encourage the exploration of emerging technologies or alternative approaches, opening new areas in the field. The research agenda of IPs should integrate basic and foundational research (e.g. computational models, architectures), component-based research (e.g. compilers, operating systems) and systems engineering and integration.

Additionally, actions targeting SME embedded tool developers and vendors are encouraged, and consequently the participation of technology brokers (e.g. associations of SMEs or technology transfer centers) in IP consortia is welcome.

Another important challenge in this domain is the *availability of skills*: properly trained design and system architecture teams that are able to think at the global system level, including the interaction with the physical environment, while making a connection to the embedded platform design. It is expected that IPs will specifically address this need.

Up to date information is available at http://www.cordis.lu/ist/so/embedded-systems/home.html

If you require further clarification, do not hesitate to contact me.

Closing date: 21 September 2005 at 17:00 Brussels local time! ■

Mercè Griera-I-Fisa (Merce.Griera-i-Fisa@cec.eu.int)

HiPEAC '05 conference

November 17-18, 2005, Barcelona, Spain

We are happy to announce HiPEAC'05, the first International Conference on High Performance Embedded Architectures & Compilers. The conference will provide a high-quality forum for computer architects and compiler builders working in the field of high performance computer architecture and compilation for embedded systems. The conference aims to achieve the dissemination of advanced scientific knowledge and the promotion of international contacts among scientists from academia and industry. The conference is open to all researchers in our community.

The first HiPEAC conference will be held in Barcelona, Spain right after MICRO-38, so that people can attend both conferences. The call for papers and the list of important dates are on the conference website: http://www.hipeac.net/hipeac2005.

We encourage everybody, and HiPEAC members in particular, to submit their best papers to the conference in order to establish the conference as a high quality event. If we succeed in making the HiPEAC conference one of the top conferences in the high performance embedded architecture and compilers area, it will become a focal point for the network members and contribute significantly towards durable integration.

Held in conjunction with the HiPEAC conference, a general HiPEAC assembly will also take place. ■

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Tom Conte, North Carolina, USA
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Steering committee

- Michiel Ronsse joined the HiPEAC network as technical support staff. Michiel graduated in 1994 as an electro-technical engineer from Ghent University. He holds a PhD in computer science, awarded in 1999. He is currently involved in the development of the HiPEAC website, the HiPEAC newsletter, the Summer School and the conference.

- Results of the first Cluster Call: 22 projects were submitted, 17 were accepted, 4 were postponed and 1 was rejected. The accepted projects are:

Coordinator	Title	Amount granted
Edinburgh University	Adaptive Optimisation	51120
RWTH Aachen	Compiler and simulation platforms	3000
University of Cyprus	Process Migration in Multi-Core Processors and its application to the Power Density Problem	17150
UPC	Collaboration on Multithreading processor design	6000
University of Patras	Adaptive Prediction Techniques for branching, prefetching, and coherence	4000
UPC	Kilo-instruction Multiprocessors	10000
University Politecnica de Valencia	CMP and low power	4000
University of Pisa	Adaptable Computers for Embedded Applications	5000
FORTH	Scalable System Architectures	10000
Chalmers	Accurate and Complexity-Effective Coherence Predictors	7880
UPC	Simulation Tools for On Chip SMT Multiprocessors	10000
UPC	Intelligent Checkpointing for Kilo-instruction Processors	20000
University of Pisa	Multicore Embedded System Architecture	8000
University of Siena	Adaptable Computers for Embedded Applications	16000
TU Delft	Automatic synthesis of Application Specific Instruction-set Processors	7000
UPC	System-level Software Optimization	4000
University of Crete	Embedded system miniaturization and power autonomy	6000
Total		189150

A presentation of HiPEAC Spain

History shows a grand tradition of Spanish contribution to the development of our field. For example, an early contributor was Ramon Llull (1231-1316), a theologian, poet, philosopher, and missionary who may have been the first person in the history of formal logic to use a mechanical device to generate (so-called) logical proofs!
Probably the most influent Spaniard was Leonardo Torres Quevedo (1852-1936), who graduated from the School of Engineering in 1876. In addition to solid work in transportation (for instance, in 1905 he built the first Spanish dirigible, and 1916 saw the first use of his cable-car at Niagara Falls, which operates to this day), he pioneered the field of automatic computing machines.
In the 1890's he created several algebraic equation solvers, in 1903 he patented the first system for remote control wireless telegraph, and in 1912 he created an electromagnetic chess playing machine (which played a flawless endgame with rook-and-king against lone king).

Another Spanish pioneer was Ramon Verea. In 1878, while living in New York, he invented a calculator with an internal multiplication table; this was much faster than the shifting carriage or other digital methods. Unfortunately, he was not interested in putting it into production, but just wanted to show that a Spaniard could invent as well as an American.

After the flurry of early activity came a lull, and from the 40's up to the 80's almost no Spanish university or company had significant influence on the development of computer architecture and compilers. In the 1970's, the Spanish national phone company (Telefónica) created the first public data-network in Europe. Subsequently, Telefónica decided to build a multicomputer specialized for packet switching. It was named TESYS (TElefónica, Secoisa Y Sitre) and, during its time was one of the most important examples of Spanish technology in the information technology field.

In the late 70's, several computer-science schools were created in Spain, followed by the establishment of research groups. In the 80's, these groups grew and started collaborations with foreign research groups.

In the 90´s, these research groups were instrumental in the creation of several supercomputing centers in Spain (CEPBA, CESGA, CESCA,...). The goal of these centers was to offer supercomputing resources to the research community, and act as a development centre for computing technology products useful to industry. In 2000, IBM joined forces with CEPBA and formed the CIRI facility (CEPBA-IBM Joint Lab) in Barcelona, to strengthen relationships between IBM and Spanish computer architecture researchers.

Currently, Spain is the attractive location for several world leading computer architecture companies that have installed research labs directed and comprised (almost completely) of Spanish engineers. In 2000, Compaq's Vax Systems and Servers Advanced Design division (VSSAD) established a laboratory in Barcelona (BSSAD) to benefit from the experience of Spanish researchers in processor design. In 2002, with the acquisition of Alpha technology by Intel, the Compaq lab became an Intel lab, and was expanded to include an advanced research group in their Microprocessor Research Labs division (MRL), in addition to the advanced development group that already existed.
As of 2004, one of the world's most powerful computers is located in Spain. It is named MareNostrum (the name that latin people gave to the Mediterranean sea), and was designed by IBM.

The High Performance Computing research group of the Computer Architecture Department at **Universitat Politécnica de Catalunya** is the one of the world's top research groups in topics related to high performance processor architectures, runtime support for parallel programming models, and the performance tuning of applications for supercomputing. Over the last 5 years, the group has published over 250 papers in refereed international conferences, and 20 PhD thesis. Former members of the group are leading Spanish universities and research groups in Intel and HP. The group has organized most of the top conferences on computer architecture (ICS'95, ISCA'98 and PACT'01) and now is organizing MICRO'05 and the first HiPEAC conference.
People: **Mateo Valero, Eduard Ayguadé, Marisa Gil, José María Llabería, Josep Llosa, Xavier Martorell, Enric Morancho, Nacho Navarro and Àlex Ramírez.**
http://recerca.ac.upc.edu/CAP/hpc/

The main research of the Computer Architecture Research Group at the **University of Cantabria** is oriented toward the design and evaluation of parallel computers. The group has contributed to interconnection network topologies, message router architectures, memory hierarchies and fault tolerant routing mechanisms. One important current direction is the proposal of suitable interconnection mechanisms to be used in on-chip multiprocessors and SoC technologies, providing scalable high-performance parallel systems at affordable cost. The group has been involved in several ESPRIT projects like "Parallelization of Wave Simulation" (PARAWAS), "Asynchronous circuit design" (ACiD-WG), "Spanish Awareness Campaign" (SAC), and others.
People: **Ramón Beivide**
http://www.atc.unican.es/

The Computer Architecture Group at the **University of Santiago de Compostela** is performing research both in software and hardware. The software research areas include high-performance software development and parallelism applications (semiconductor device simulation, computer graphics, meteorology,...), compilation techniques and performance analysis of parallel computers, and grid computing. Hardware research focuses on processor design, computer arithmetic and processors for image and video processing. This group cooperates with several European and American groups.
People: **Javier Díaz Bruguera**
http://www.ac.usc.es/

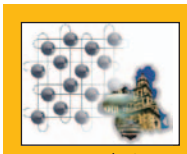
MareNostrum is ranked fourth in the latest update of the Top-500 list of the world´s most powerful computers, and is ranked first amongst those located in European countries. MareNostrum´s performance is quite impressive: 40 TeraFlops at peak speed and 320 Terabytes of hard-disk capacity. MareNostrum and the Barcelona Supercomputing Center (www.bsc.es) will help the international scientific community to devise and conduct much more ambitious projects.

To sum up, Spanish researchers have been working hard during the previous decades and will continue to do so. Consequently, we strongly believe that they will have significant influence on the development of high performance embedded architectures and compilers. ■

The research interests of the GAP (Parallel Architectures Group) at the **Universidad Politécnica de Valencia** include numerous topics related to interconnection networks. The most relevant results of the group are a theory and design methodology to guarantee the absence of deadlock in networks using adaptive routing and a scalable congestion management technique for lossless networks. The former has been used in the MIT Reliable Router, the Cray T3E supercomputer, the on-chip router in the Alpha 21364 microprocessor, the Cray Black Widow supercomputer, and the IBM BlueGene/L (currently the world's most powerful supercomputer). The latter will be implemented in the future generation of high-performance switches from Xyratex, and is being considered for inclusion in the standard for PCI-Express Advanced Switching (ASI).

People: **José Duato**

http://www.gap.upv.es/



The main research interests of the GACOP (Parallel Computing Architecture) Research Group at the **University of Murcia** are micro-architecture, parallel architectures, interconnection networks and grid computing. More precisely, branch and value prediction for superscalar/multithreaded architectures, low power techniques for HPC/embedded processors/CMPs, scalability techniques for cc-NUMAs, and efficient cache-coherence protocols for CMPs. GACOP provides expertise in low-level communication protocols for the Quadrics clusters. GACOP has collaborated with Los Alamos National Laboratory to develop tools (job launching and scheduling of MPI applications), and communication libraries (BCS-MPI).

People: **José Manuel García**

http://ditec.um.es/gacop/

The activities of the research group at the **University Autónoma of Barcelona** (UAB) during the last years have been in the design of a fetch unit that balances low latency and high instruction bandwidth; this design is targeted at superscalar and SMT processors, and chip multiprocessors. The group has initiated research on dynamically adaptable designs that improve the performance of the cache and fetch unit, with an efficient use of area and power, in collaboration with the University of Las Palmas de Gran Canaria. Other research interests include improving communications in interconnection networks. The group´s main contributions are the development of scalable and fully distributed mechanisms for traffic load balancing, with the aim of avoiding network hot-spots.

People: **Emilio Luque**

http://dept-inf.uab.es/

The gaZ (Computer Architecture Group at the **University of Zaragoza**) works jointly with the High-Performance Computer Architecture group of the UPC in issues related to on-chip memory hierarchy for high-performance processors. Some of our contributions are policies for reducing the size of the register file through a careful control of (delayed) register allocation and (early) release, multibanked first-level data cache designs able to give both low latency and high bandwidth, speculative state management in thread-level speculative multiprocessors (with Illinois University), and pattern-directed hardware data prefetching. Recently we have also started on multiprocessor coherency prediction (with Chalmers University of Technology).

People: **Víctor Viñals**

http://webdiis.unizar.es/gaz/

The ArTeCS (Architecture and Technology of Computing Systems group at the **Complutense University of Madrid**) group focuses on the conception of new high-performance computing systems, in conjunction with efficient exploitation of processing speed, energy consumption and cost. The main working areas of ArTeCS are: a) Processor Architecture (increasing processor performance), b) Algorithms and methodologies to efficiently exploit new architectural proposals (computational power issues associated with bioinformatics and computational biology), and c) High-performance embedded systems (creation of hardware/software solutions that allow architects to deal with the complexity of applications, and their power dissipation constraints and performance requirements).

People: **Francisco Tirado**

URL: http://atc.dacya.ucm.es/

The Department of Computer Architecture at the **University of Málaga** comprises a total of 35 members. The main research of the group is concerned with high-performance computing, providing solutions for efficient programming, improving processor architectures, and exploring new algorithms for image processing, multimedia, and physical/biological system modeling. To this end, we have developed parallelization and optimization techniques at the language, compiler and runtime levels, specially for sparse, irregular and pointer-based codes; solutions for numerical, graphical and audiovisual (multimedia) computations at the application and architecture levels; and system architectures for bioinformatics, VoD and massive storage.

People: **Emilio L. Zapata, Óscar Plata**

URL: http://www.ac.uma.es/

PhD news

Stating and Manipulating Periodicity in the Polytope Model. Applications to Program Analysis and Optimization

by Benoît Meister, meister@icps.u-strasbg.fr, ICPS/LSIIT, Université Louis Pasteur, France, December 2004

This thesis focuses on mathematical objects that are the intersection between a rational parametric polyhedron and a lattice of integer points: Z-polyhedra. The main contribution of this thesis is an enhancement of the polyhedron model, by integrating the periodic character of extremal integer points of the Z-polyhedron, using "periodic polyhedra". This concept is first used to devise the first algorithm for computing the integer hull of a parametric Z-polyhedron P, i.e., the convex hull of the integer points that belong to P.

Storage Bandwidth optimization for dynamic multi-threaded applications

by Paul Marchal, paul.marchal@imec.be, IMEC, Leuven, Belgium, January 2005

In this PhD, we present an integrated data assignment/task scheduling technique to reduce the cost of the shared SDRAMs. We also introduce "loop morphing" for globally reorganizing the memory accesses to the local memory layers. In addition, we propose a scenario-based approach to cope with the dynamic behavior. Finally, we discuss a configurable memory manager and DMA-capable memories for efficiently enforcing data-assignment decisions at run-time. Experiments indicate that our techniques significantly improve the performance or reduce the energy cost of dynamic multi-threaded applications.

A coarse-grained reconfigurable architecture template and its compilation techniques

by Bingfeng Mei, bingfeng.mei@imec.be, IMEC, Leuven, Belgium, January 2005

In this thesis, a novel Coarse Grained Reconfigurable Architecture, ADRES (architecture for dynamically reconfigurable embedded systems), and a compiler framework, DRESC (dynamically reconfigurable embedded system compiler), are presented. Our approach possesses several unique features. The ADRES architecture tightly couples a very-long instruction word (VLIW) processor and a coarse-grained array by providing two functional views on the same physical resources. Second, the DRESC framework introduces software-like design experience. A multimedia application, MPEG-2 decoder, is mapped within one week starting from a software implementation. The speed-up over an 8-issue VLIW is about 12 times for kernels and 5 times for the entire application.

in the spotlights

ISS devises novel micro-profiling technology for application specific processor design

RWTH AACHEN UNIVERSITY

Application specific instruction-set processors (ASIP) provide a good compromise between flexibility and energy efficiency in embedded system design. Architecture exploration is required to fine-tune a processor for a given application. This exploration is supported by the LISA processor modeling language and the associated LisaTek tools developed at ISS. They allow for automatic generation of the complete software tool chain from an ASIP model, comprising assembler, linker, simulator / debugger, and C-compiler, as well as HDL synthesis models. Using LISATek the designer can quickly perform architectural optimizations once the "hot spots" in the application code are known. Finding those hot spots that deserve special hardware support requires extensive code profiling. ISS's new processor-independent micro-profiler (µP) combines C-level profiling efficiency with high accuracy. The µP translates ANSI C code into an executable low-level C format, whilst automatically inserting probes for fine-grained code instrumentation. The instrumented code can be compiled on an arbitrary platform (e.g. with gcc). Code execution then gathers precise statistics, including dynamic application characteristics not visible with classical C/C++ profilers.

In addition, highly accurate source-level data cache profiling is supported. The µP provides a GUI for visualizing the statistics in different formats. Thereby, it guides an ASIP designer in making the right early architectural decisions during ISA design and memory architecture exploration. Furthermore, the micro-profiling data can be forwarded to a tool for automatic synthesis of application specific instruction patterns. Finally, using a rudimentary retargeting mechanism, the µP allows for early and accurate performance estimation for partially defined processor architectures. Thus, the µP serves as a "pre-architecture" exploration tool before model-based ASIP micro-architecture exploration. It is available for research purposes on request. ■

About ISS

The Institute for Integrated Signal Processing Systems at RWTH Aachen University of Technology focuses on the design of wireless communication systems. A number of successful design automation tools for application specific systems have been developed at ISS, with LISATek (now available from CoWare Inc.) being the most recent example. Current research activities concentrate on multi-processor SoC design and exploration, and compilers for embedded processors.

Further information can be found at http://www.iss.rwth-aachen.de.

Prof. Rainer Leupers, leupers@iss.rwth-aachen.de

ACACES'2005: International summer school on advanced computer architecture and compilation for embedded systems

July 24-30, 2005 L'Aquila, Italy

We are proud to announce the first HiPEAC Summer School, which will take place in L'Aquila, a small town about 100 km northeast of Rome. L'Aquila is the capital town of Abruzzi and of the Province of L'Aquila. The event will be held at the Telecom Italia Learning Services Campus, located on a small hill a few kilometers away from the center of L'Aquila.

A distinguishing feature of this Summer School is its broad scope ranging from low level technological issues to advanced compilation techniques. In the design of modern computer systems one has to be knowledgeable about architecture as well as about the quality of code and how to improve it. This summer school offers the ideal mix of the two worlds – both at the entry level and at the most advanced level. The summer school is open to everybody, but previous training and/or experience in computer science as well as a strong background in computer architecture or compilation is recommended.

The steering committee has succeeded in setting up a truly remarkable program. We start on Sunday evening with Prof. Maurice Wilkes who will address the summer school during the opening ceremony. On Monday, the 12 courses start spread over two morning slots and two afternoon slots. Per slot there are three parallel courses of which you can take one. The courses have been allocated to slots in such a way that it will be possible to create a summer school program that matches your research interests. The topics of this year's Summer School will be presented by **world-class experts** from both industry and academia.

On **Monday evening** there will be an invited talk by Jim Kahle, IBM fellow and chief architect of the Cell processor.

On **Tuesday evening** we have organised a poster session where the participants can present their own work to the other participants in order to foster interaction and future collaboration.

On **Wednesday afternoon** there will be a half day excursion to the splendid gardens of Villa d'Este. Villa d'Este is a UNESCO World Heritage site.

On **Thursday evening** there will be a panel discussion on a hot topic in computer architecture and compilation.

On **Friday evening** there is a farewell dinner.

We have really tried to make the summer school a memorable event. Students and lecturers will be accommodated in hotel-standard private rooms on campus, where they will stay one week. This will provide plenty of opportunity to have discussions with the teachers and with the other participants in the relaxing surroundings of the Telecom Italia Learning Facilities Campus. Long after-the-lecture discussions at the bar or the pool table will be one of the major assets of this summer school. At the end of the event you will receive a certificate of attendance detailing the courses you took.

You can arrange to be picked up in Rome on Sunday July 24, 2005 and taken back on Saturday July 30, 2005 to either Rome airport or downtown Rome (for those who want to spend some extra time in the eternal city). We will take care of everything during the full week for only 990 euro, a very reasonable price for an event of this quality.

Unfortunately, the number of partipicants will be limited. Therefore, we have an admission procedure to guarantee a fair distribution of the available places among all qualified applicants from the various countries and institutions. In case of conflict, preference will be given to the participants who filed their application earlier, so don't wait too long to fill in your form. If you are a member of a HiPEAC institution you can ask for a grant that covers the registration fee.

In this newsletter, you will find a summer school poster. Please post it at some visible place in your department.

You can find more information about the summer school at http://www.hipeac.net/summerschool.

We look forward to seeing you there!
Koen De Bosschere
Summer school organizer ■

Lecturer	Course
David August, Princeton University, USA	Simulation
Doug Burger, University of Texas at Austin, USA	Tiled architectures
José Duato, University of Valencia, Spain	High-speed interconnection networks
Josh Fisher, HP, USA	High performance embedded computing
Rajiv Gupta, University of Arizona, USA	Compilation for embedded processors
Avi Mendelson, Intel, Israel	Low power
Trevor Mudge, University of Michigan, USA	Memory systems and their implementation technologies
Mike O'Boyle, University of Edinburgh, UK	Adaptive & feedback driven compilation
Yale Patt, University of Texas at Austin, USA	Advanced microarchitecture
Jim Smith, University of Wisconsin-Madison, USA	Virtual machines
Per Stenström, Chalmers, Sweden	Chip multiprocessors
Olivier Temam, INRIA Futurs, France	Simulation
Ayal Zaks, IBM, Israel	Optimizations in GCC

Upcoming events

CF '05, 2005 ACM International Conference on Computing Frontiers
Ischia, Italy, 4-6 May 2005, http://www.computingfrontiers.org

Course: Memory Technologies for Future System Design (SOC-32),
IMEC, Leuven, Belgium, May 30, 2005, http://www.imec.be/mtc/Memory-Technologies.htm

ISCA 2005, The 32nd Annual International Symposium on Computer Architecture
Madison, Wisconsin USA, June 4-8, 2005, http://www.cs.wisc.edu/~isca2005

PLDI 2005: Conference on Programming Language Design and Implementation
Chicago, June 12-15, 2005, http://www.research.ibm.com/pldi2005

ICAC 2005: International Conference of Autonomic Computing,
Seattle, WA, June 13-16, 2005, http://www.caip.rutgers.edu/~parashar/icac2005/index.htm

DAC 2005: Design Automation Conference, Anaheim Convention Center
Anaheim, CA, June 13-17, 2005, http://www.dac.com/42nd/index.html

PPoPP 2005: Conference on Principles and Practices of Parallel Programming
Chicago, IL, June 15-17, 2005, http://www.cs.cornell.edu/Conferences/PPoPP05

LCTES 2005: Conference on Languages, Compilers, and Tools for Embedded Systems
Chicago, IL, June 15-17, 2005, http://lctes05.snu.ac.kr

SAMOS V: Embedded Computer Systems: Architectures, MOdeling, and Simulation
Samos, Greece, July 18-20, 2005, http://samos.et.tudelft.nl/samos_v/

HiPEAC Summer School on advanced architectures and compilation for embedded systems
L'Aquila, Italy, July 24-30, 2005, http://www.hipeac.net/summerschool/

Euro-Par 2005,
Lisbon, Portugal, August 30 - September 2, 2005, http://europar05.di.fct.unl.pt/

PACT-2005: The Fourteenth International Conference on Parallel Architectures and Compilation Techniques
Saint Louis, Missouri, September 17-21, 2005, http://pact05.ce.ucsc.edu/

CODES+ISSS 2005: International Conference on Hardware - Software Codesign and System Synthesis
New York, September 19-21, 2005, http://www.codes-isss.org/

PATMOS 2005: International workshop on Power and Timing Modeling, Optimization and Simulation
Leuven, September 20-23, 2005, http://www.imec.be/patmos/

MICRO-38: The 38th Annual IEEE/ACM International Symposium on Microarchitecture
Barcelona, Spain, November 12-16, http://pcsostres.ac.upc.edu/micro38/

HiPEAC '05 Conference
Barcelona, Spain, November 2005, http://www.hipeac.net/hipeac2005/

If you are a HiPEAC member, and you want to contribute to this newsletter, please contact Michiel Ronsse at Michiel.Ronsse@elis.UGent.be

HiPEAC info 2
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A presentation of HiPEAC UK