



Thales Research & Technology Embedded System Lab - France

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- High performance Embedded systems and tools for Aerospace, Defence and Security application
- Signal processing application
 - Radar, Sonar, Electronic Warfare applications
 - Telecommunications
 - “Data flow” dominant with real time constraint and high reactivity requirements
- Image processing application
 - Video surveillance
 - Motion detection and pattern (facial/intruder) recognition
 - Fine grain massively parallel SIMD processing



50 %

Defence



Security

25 %



Aerospace

25 %

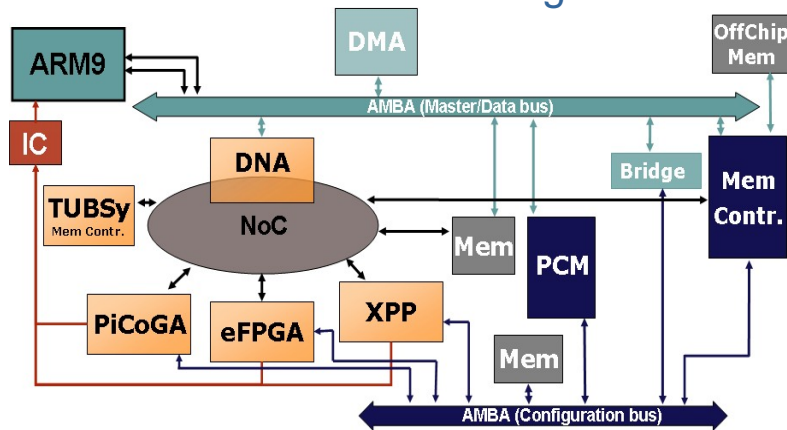


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Some Current Projects

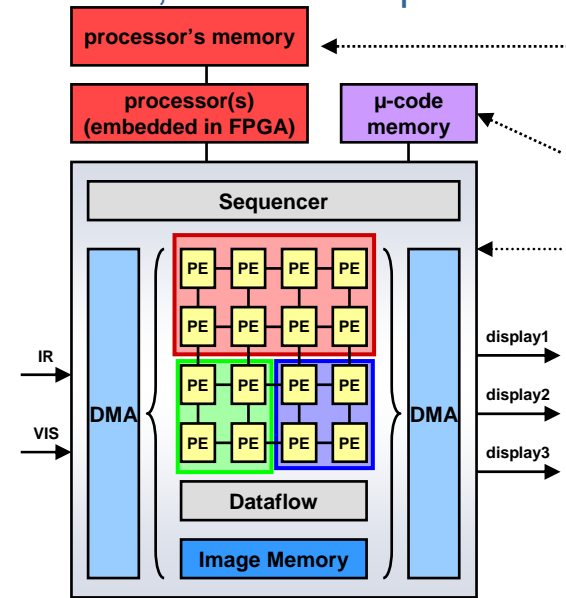
■ Morpheus

- Multi-purpose dynamically Reconfigurable Platform for intensive Heterogeneous processing
- IP : EU 6th Framework Program IST

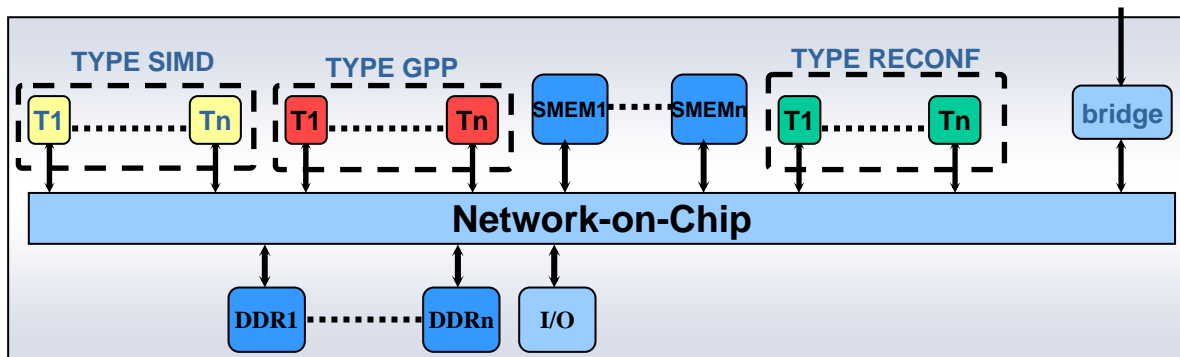


■ Ter@core: SIMD for image processing

- 128 PEs, ~20 GOPS peak 150 MHz



■ Ter@ops: MPSoC for stream processing dominant applications



- Multi-domain
- High Level of SW productivity
- High GOPS/W (respect to GPP)
- Project started in 2007

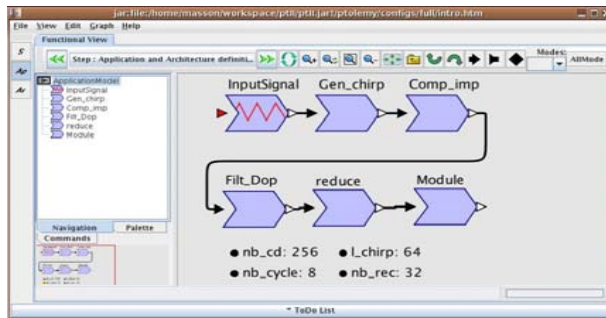
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SPEAR Application Development Framework

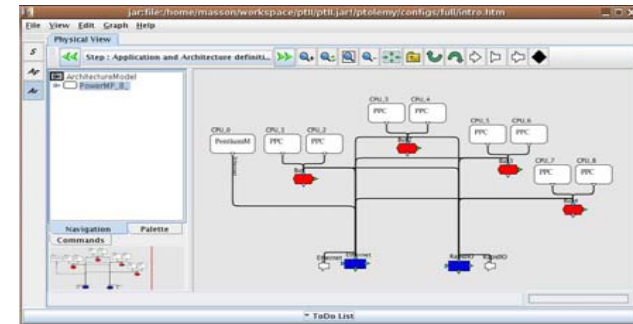


- Captures both application and architecture
 - Application modelled as acyclic graphs of tasks, Heterogeneous architecture
- Supports application partitioning/mapping, communication insertion, scheduling
 - Mapping is human-driven - enables iterative design exploration

Application Capture

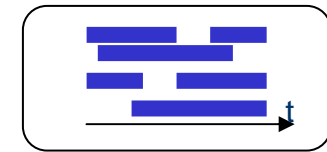
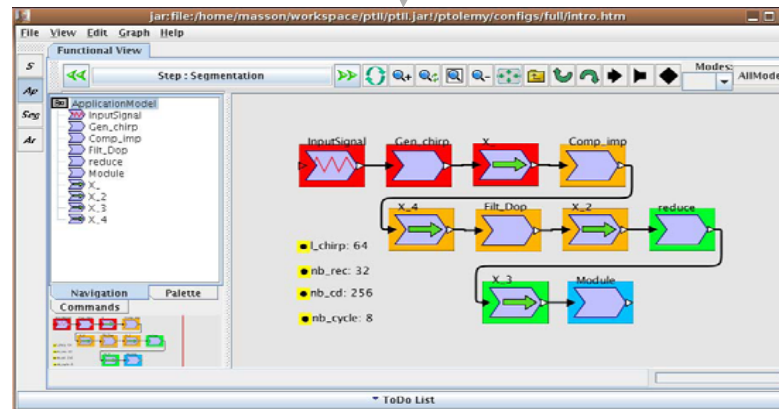


Architecture Capture



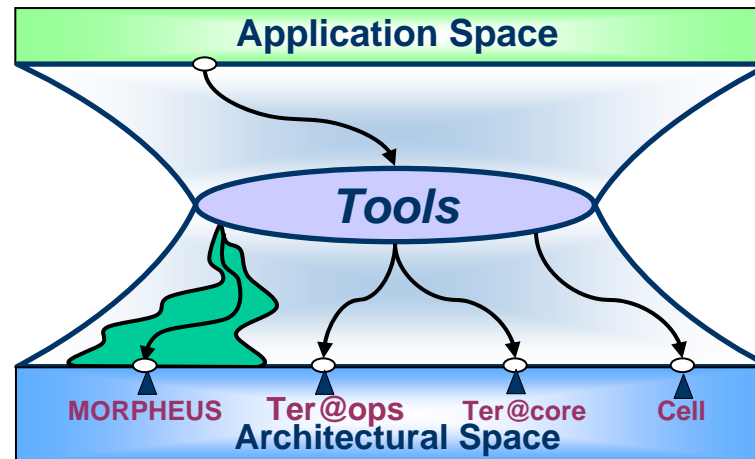
Mapping

Code Generation



Performance Simulation

Diversity of THALES applications distributed in Business Units



Diversity of architectural solutions

■ Specialization: how to parallelize ?

Parallelism

- Use of existing programming models
- Homogeneous processing and load/task distribution



Specialization

- Efficiency
- Performance

⇒ Multipurpose multi-faceted solutions for cost effective specialization

- HW reconfiguration, polymorphic programming model, etc
- Benchmarking and workload characterization
 - (bench suite for signal and image processing?)
- Multicore & system simulation acceleration using FPGA