
Programming models and operating systems (PRO) cluster

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Cluster meeting agenda

- Welcome
 - Purpose: identification of opportunities for joint work, technology sharing and possible EU projects
 - Membership: 40 → 54 members
 - Events
- PRO roadmap status
- Short presentations (4 x 10' each)
- Mini-tutorial (20')
- Upcoming FP7 Call 4
- Closing

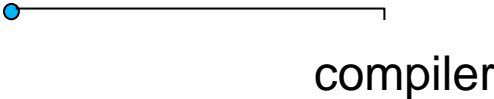
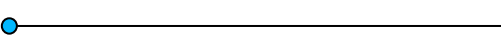
PRO-related events

- MULTIPROG-2009 workshop
 - Joint event with the Multicore Architecture cluster
 - In conjunction with HiPEAC-2009
 - Less submissions than MULTIPROG-2008 (12)
 - Currently deciding accepted/rejected papers
 - Ideas/proposals for filling program

PRO roadmap (1/6)

- Vision 2012-2020: identify where to go and the main challenges/problems in going there
 - Led by Marc Duranton of NXP
 - Draft already available
 - It will be visible through cluster webpage
 - Your comments and contributions are really welcomed
 - PRO part very biased with BSC/UPC's vision ... shouldn't be!
 - A first version is due mid-january

PRO roadmap (2/6)

- Expressing vs. exploiting parallelism in a scenario with more and more resources (number and heterogeneity) and applications that not necessarily fit the HPC domain, looking for the appropriate support from the underneath architecture, compiler and OS
- Three main areas identified
 - Programming models 
 - Runtime systems 
 - OS/architecture interfaces and support

PRO roadmap (3/6)

- Programming models:
 - Semantics/productivity trade-off
 - Ease programming for heterogeneity
 - Transparent data access in shared address space (data movement, software caches, NUMA domains, ...)
 - Development environments (automatic parallelization, program transformation, debugging, performance analysis and prediction)
 - Interoperability with other non-shared memory programming models and target compilers

PRO roadmap (4/6)

- Runtime systems:
 - Autotuning: granularities and amount of parallelism (loop scheduling, task scheduling, ...)
 - Dynamically handling of resource heterogeneity: systems with slow/fast, simple/complex, domain accelerators (e.g. cell, gpu), application accelerators (e.g. fpga), ...
 - Transparent and dynamic load balancing: application, resources, multiprogramming
 - Power/temperature-aware decisions (e.g. scheduling)

PRO roadmap (5/6)

- OS/architecture interfaces and support
 - Hardware support to programming model and runtime system (hw-acceleration or providing new abstractions), revisiting instruction-sets, ...
 - Scalable (up/down) interfaces to handle heterogeneity
 - Kernel-level support for resource adaptability (e.g. load balancing, thread priorities, ...)
 - Mechanisms for non-intrusive observation of application execution (program tracing and autotuning)
 - Interaction with virtualization: performance isolation, quality of service, interference/cooperation among schedulers, ...

PRO roadmap (6/6)

- Draft will be made available through cluster webpage
- Your comments and contributions are welcomed ... it's time for brainstorming and un-biasing from BSC/UPC's vision

List of presentations

- Avi Mendelson, Intel and Technion (Israel)
 - Making Streaming mainstream
- Enrique Quintana-Orti, U. Jaime I (Spain)
 - Extending the StarSs programming model for platforms with multiple hardware accelerators
- Lefteris Polychronopoulos, U. Patras (Greece)
 - Parallel and distributed systems group
- Patrick Viry, Ateji (France)
 - Language technologies for parallel computing
- Xavier Martorell, BSC and UPC (Spain)
 - S2S program transformations with the Mercurium compiler

Upcoming FP7 call 4 (1/2)

Challenge 3 “Components, systems, engineering”, Objective ICT-2009.3.6 “Computing Systems”

- Parallelization and programmability
- Methodologies, techniques and tools
- System simulation and analysis
- Technology implications

Projects on programmability and parallelism of homogeneous or heterogeneous multi-core and/or reconfigurable architectures should adopt a **holistic** approach addressing issues related to the underlying hardware, the operating system and the system software.

- Instruments: STREPS (24.7 M€), CSA (0.3 M€)

Upcoming FP7 call 4 (2/2)

Future and Emerging Technologies FET proactive, Objective ICT-2009.8.1 “Concurrent Tera-device Computing”

- Radically new methods and tools for architecture design and programming of chips and systems **beyond 2020**, including compilers and run-time systems:
 - Complexity of design and run-time of many-core heterogeneous systems
 - Design of dependable systems with faulty components
 - Breakthrough programming paradigms

The developments should be motivated by the requirements of wide classes of **relevant applications** in a time scale of 10-15 years.

Integrated projects should address at least two of the above topics, STREPs at least one.

- Instruments: IP, STREP. 15 M€, of which a minimum of 50% to IPs

Closing

- Any Call For Partners in the room? Or Call For Discussion on a specific research topic?

Thanks for attending
and contributing!

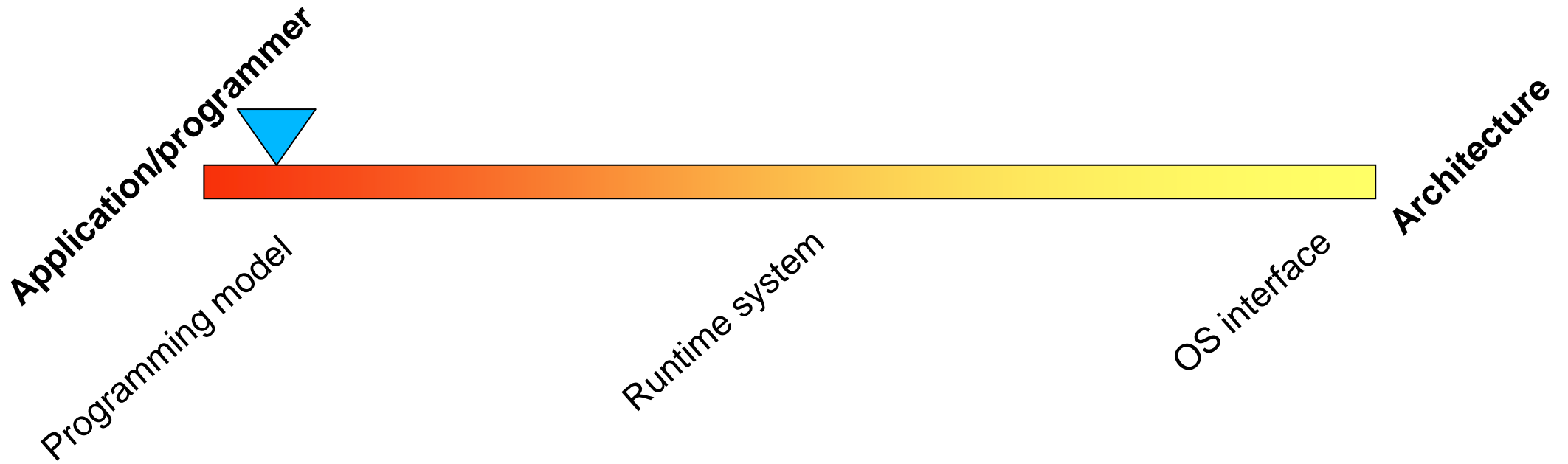
Multicore cluster

- facilitate collaborations between academic and industrial nodes: consortia formations
 - successful consortia must cut across multiple clusters → holistic approach
 - should target a broad spectrum of applications
 - call for partners
- creating a roadmap: long-term research agenda in programming models
- linking research activities with those of other clusters and contribute to taskforces

Adaptive compilation

- cluster collaboration grants
 - for collaboration between cluster members
 - 15 Ke budget per year (money for site visits to perform joint research)
- roadmap

PRO roadmap (2)



gcc with stm

- flat nesting
- tinySTM
- weak isolation
- tm_callable and tm_pure
- Red Hat Richard Henderson
 - __tm_atomic keyword instead of pragama
 - targets intel ABI

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- Institute for System Programming of the Russian Academy of Sciences (ISP RAS)