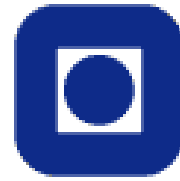


NTNU, Trondheim, Norway

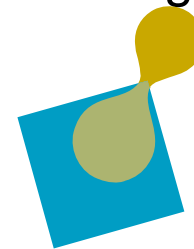


NTNU
Norwegian University of
Science and Technology

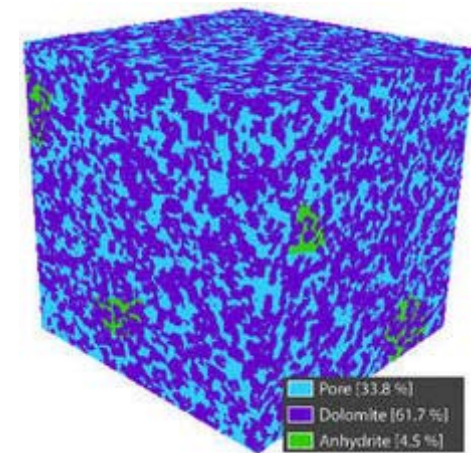
- **NTNU (Trondheim, Norway)**
- **Lasse Natvig**
 - Professor in computer architecture
 - Department of computer and information science (IDI), NTNU
- **Possible collaboration areas within prog.mod.& OS cluster**
 - 1) General purpose hardware acceleration in HPC Clusters, with Numerical Rocks
 - 2) Parallelization of Linear Programming (LP) on Novel Multicore Hardware, with Miriam AS
 - 3) Efficient and portable parallel programming (EU 7FP, call 4 ...)
- **Related activity**
 - Cooperating with Dr. Anne Elster's HPC group at NTNU
 - Simulation based design space exploration of multicore memory systems (Participating in the multi-cluster)

1) Numerical Rocks, HPC and CUDA?

- **Context:** Objective: compute representative petrophysical and transport properties of reservoir rocks directly from 3D images of the rock microstructure. (oil&gas industry)
- Development of highly optimized massively parallel algorithms running on HPC clusters using state-of-the-art acceleration boards from the HPC and gaming industry.
- Candidate platforms: GPUs, physics processing units (PPUs), Cell BE and homogeneous multicore processors
- Status: PhD-student B. M. Mathisen
 - PhD courses, initial experiments with **CUDA and an 8-core workstation, Tesla**
 - Participates at ICS, Greece, 7-12 June.
 - Co-supervisor is Dr. Anne Elster
- Collaboration:
 - similar projects?
 - 3 – 6 months stay in a relevant research group



numericalrocks



2) LP parallelization on Cell



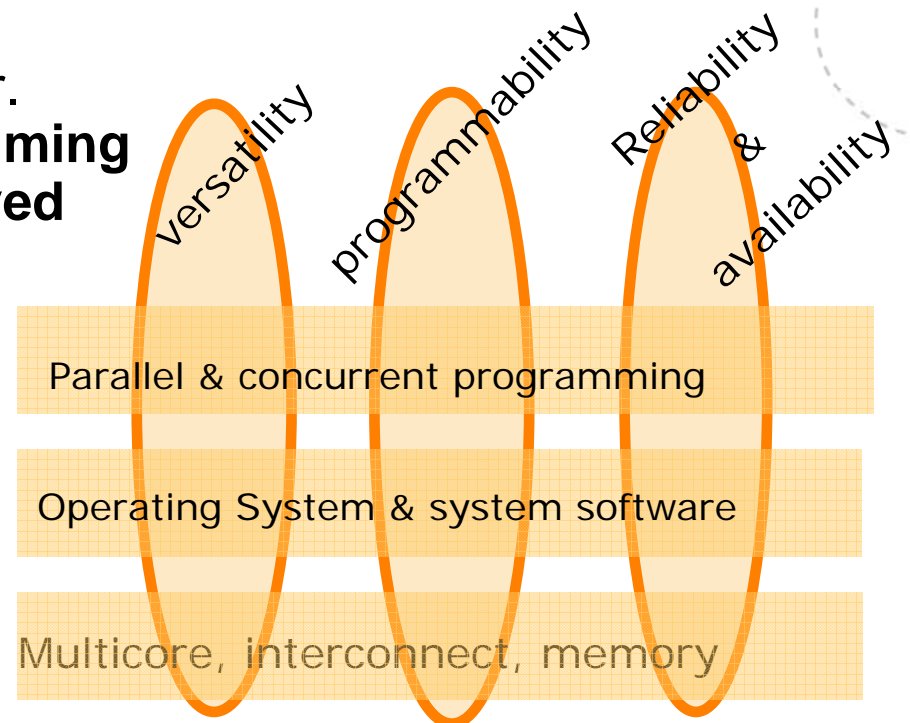
MIRIAM

GAS SIMULATION AND FORECASTING CENTER

- **Context:** Miriam Gas Simulation and Forecasting Centre in Halden, Norway, develops a gas network simulation system. To be able to better support the European gas market increased computational performance is required.
- Miriam AS in cooperation with NTNU has very recently got an “**industry-PhD**” **fellowship** focused at parallelisation of Linear Programming (LP) on Novel Multicore Hardware.
- **Platform:** A cluster of **Cell Broadband Engine**
- **Main challenge:** Adopt a layered parallelisation approach to make the software more robust to future changes in the underlying compute platform, i.e. to combine high computational efficiency with software portability.
- **Status:** Need applications NOW, deadline 13 June 2008.
- **Collaboration:** yes

4 3) Efficient and portable parallel programming (EU 7FP, call 4 ...)

- Partner in a STREP proposal spring 2007 for **EU 7FP challenge 3.4** --- programmability of multi-core systems.
 - No. 13 of 24 ? (Above all thresholds, low budget)
 - Coordinator: Univ of. Vienna
- We want to take part in STREP proposals etc. as a research partner. Possible role: **“linking the programming level to the HW to achieve improved performance”**. **Holistic view** on multi-core application performance.



Background & contact info

- Background for research in multicore programming
 - PhD: "Evaluating Parallel Algorithms: Theoretical and Practical Aspects " (1991)
 - Simulation of the P-RAM model, Synchronous MIMD programming, Simulation of Valiant's BSP model, general interest in HW/SW interface, parallelism, and simulation based research in multicore memory systems (since 2004)
- **Contact:**
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