Overview of Tutorial on Design Variability

Micro-41

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Technology Outlook

- Technology scaling continues as normal
- Delay scaling will slow down
- Energy scaling will slow down
- RC Delay constant
- Variability: will increase dramatically

Sources of Variability

PROCESS	Cct Operation	Simulation Tools
Channel Length	Temperature	Timing Analysis
Channel Width	Supply Voltage	RC Extraction
Threshold Volt.	Aging	Cell Modelling
Overlap Cap.	Cross Coupling Capacitance	Circuit Simulations
Interconnect	Multiple Input Switching	Transistor Models

Static Variation

- D2D
- WID
  - Systematic: long range order of mm
  - Random: short range
    - Can vary from transistor to transistor
    - Increase with scaling
- Manufacturing process imperfections
  - E.g. lens aberations, processing temperature, random dopant variations

Dynamic Variation

- Supply voltage
  - ns-100us
- Temperature Variation
  - Due to activity and ambient
  - ms for full sweep, much faster for few degrees
- Wear-out
  - Vt degrades from bias and temperature

Solutions

- Static Variations
  - Adjust supply voltage
  - Apply body-bias
  - Circuit tricks – time borrowing
- Dynamic Variations: sense and respond
  - sense: activity, temperature, voltage droop…
  - respond: body bias, supply voltage, frequency
  - Razor circuits coupled with recovery

Implications of Variations

- Increase design, manufacturing effort
- Critical path
- Leakage
- Fmax
- Binning
- Yield

SRAM

- Types of failures:
  - Timing
  - Read, pseudo-destructive read
  - Write, can not write
  - Retention failure
- Solutions:
  - Layout: Bigger cells
    - 90nm 1MB, 65nm 1.75MB, 45nm 2.89MB
  - Circuits: more transistor/cell, dynamic cells + refresh
  - Architectural Techniques

Power and PV

- Voltage scaling
  - linear performance degradation
  - cubic power reduction
- Power envelope constraints may force operation below Vcc-min

  > linear performance degradation
  - Some devices will not function correctly

  cubic power reduction