

Maria K. Michael
Assistant Professor



ECE Department
University of Cyprus
<http://www.ece.ucy.ac>



KIOS Research Center
for Intelligent Systems and Networks
University of Cyprus
<http://www.kios.org.cy>

Research Background & Interests

- ❖ Computer-Aided Design Tools and Methodologies for Manufacturing Test and Fault Diagnosis
 - ❖ CAD algorithms for automated testing (automatic test pattern generation/compaction/compression, fault simulation, testability analysis, ...)
 - ❖ Fault diagnosis (locate & characterize source of error)
- ❖ Fault Modelling
 - ❖ static/functional faults (ex. Stuck-at faults)
 - ❖ dynamic/timing (performance) faults (ex. delay and bridging faults)
 - ❖ level of abstraction: logic, RTL

Research

Background & Interests

- ❖ Design-for Testability (DFT)
 - ❖ Off-line Self-Test (test data/time reduction) – H/W BIST
 - ❖ On-line Self-Test (microprocessor test) – S/W BIST
- ❖ Semi-formal methods for logic/timing verification and analysis
 - ❖ test-based verification, symbolic techniques s.a. Boolean SAT and Binary Decision Diagrams
- ❖ Fault tolerance and Reliability
 - ❖ Logic, Architectural, S/W levels
- ❖ Applications
 - ❖ large-scale (digital) VLSI circuits
 - ❖ reusable embedded cores integrated into chip-level architectures such as SoCs, NoCs, multicores (MPSoCs, CMPs)

Recent related projects

- ❖ Software-based self-test of microprocessors
(with *Politecnico di Torino, ST Microelectronics*), 2007 --
 - ❖ Automatic generation of test programs (assembly code)
 - ❖ Target performance faults (excessive delays on critical paths)
 - ❖ Utilizes computational intelligence engine, with appropriate guidance to generate useful test programs
 - ❖ Hybrid gate- and RT-level descriptions
- ❖ System-level Intelligent Collaboration in Chip Multiprocessors
(partly supported by *Intel Corp, USA*), 2007 --
 - ❖ Dynamic process/task mapping on cores
 - ❖ Utilizes system feedback

Recent related projects

- ❖ **Reliable Next-Generation Manycore Chips**
(with *U of Bristol, Cyprus U of Technology, and SignalGX*,
funded by *Cyprus Research Promotion Foundation*), 2008 -- 2010
 - ❖ Investigate appropriate fault detection/tolerance in various components (cores, memory, network)
 - ❖ Target permanent and temporary faults (caused by initially unreliable components, ware-outs, aggressive voltage scaling, etc)
- ❖ **Energy-Efficient Embedded and Mobile MPSoC Architectures**
(with *Cyprus U of Technology and SignalGX*,
funded by *Cyprus Research Promotion Foundation*), 2008 -- 2010
 - ❖ Application specific design space exploration
 - ❖ Development of Simulation and Prototyping (FPGA-based) framework

Reliability issues for multi-cores

- ❖ Application matters! However, some type of reliability will be necessary in all (technology implications) ...
- ❖ How much redundancy (or overhead)?
- ❖ What type of redundancy (use time or space, probably hybrid...)?
- ❖ At which level should we detect/locate/tolerate (circuit, architecture, S/W)?
- ❖ Reconfigurability & Programmability