

C O N F E R E N C E P R O G R A M M E

**Sunday, 23 January**

18:00-21:00 **Registration**  
19:00-21:00 **Welcome Cocktail**

**Monday, 24 January**

9:00 - 9:15 **Opening and Welcome Remarks**

9:15-10:30 **Keynote I: Moore's Law Implications on Energy Reduction**  
*Antonio Gonzalez, Intel & UPC*

10:30-11:00 **Coffee Break**

11:00-12:30 **Paper Session 1: Parallelization & Run-Time Systems**

**A Stream-Computing Extension to OpenMP**  
*Antoni Pop (MINES ParisTech), Albert Cohen (INRIA)*

**GLOpenCL: OpenCL Support on Hardware- and Software-Managed Cache Multicores**  
*Konstantis Daloukas, Christos Antonopoulos, Nikolaos Bellas (University of Thessaly)*

**DDM-VMc: The Data Driven Multithreading Virtual Machine for the Cell Processor**  
*Samer Arandi, Paraskevas Evripidou (University of Cyprus)*

12:30-14:00 **Lunch**

14:00-15:30 **Paper Session 2: Compilers**

**Speculatively Vectorized Bytecode**  
*Erven Rohou, Kevin Williams, Albert Cohen (INRIA), Sergei Dyshel, Dorit Nuzman, Ira Rosen, Ayal Zaks (IBM Haifa Research Lab)*

**Parallel Points-to Analysis for Multi-Core Machines**  
*Marcus Edvinsson, Jonas Lundberg, Welf Löwe (Linnaeus University)*

**TypeCaster: Demystify Dynamic Typing of JavaScript Applications**  
*Shisheng Li, Buqi Cheng, Xiao-Feng Li (Intel Corporation)*

15:30-16:00 **Coffee Break**

16:00-18:00 **Paper Session 3: Memory Systems; Real-time Systems**

**Extended Histories: Improving Regularity and Performance in Correlation Prefetchers**  
*Manikantan R., Govindarajan R. (Indian Institute of Science), Kaushik Rajan (Microsoft Research India)*

**Decoupled Zero-Compressed Memory**  
*Julien Dusser, André Seznec (INRIA/IRISA)*

**High Throughput Data Redundancy Removal Algorithm with Scalable Performance**  
*Ankur Narang, Souvik Bhattacharjee, Vikas Garg (IBM Research, India)*

**RVC: A Mechanism for Time-Analyzable Real-Time Processors with Faulty Caches**  
*Jaume Abella, Eduardo Quiñones (BSC-CNS), Francisco Cazorla (BSC-CNS and IIIA-CSIC), Yanos Sazeides (University of Cyprus), Mateo Valero (BSC-CNS and UPC)*

18:00-18:10 **HiPEAC'12 Presentation**

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## Tuesday, 25 January

- 9:00-10:15 **Keynote Speech II: PetaBricks: A Language and Compiler based on Autotuning**  
*Saman Amarasinghe, MIT*
- 10:15-10:45 **Coffee Break**
- 10:45-12:45 **Paper Session 4: Optimization for multi-cores; Parallelization & Runtime Systems**
- Automated Empirical Tuning of Scientific Codes For Performance and Power Consumption**  
*Shah Mohammad Faizur Rahman, Jichi Guo, Qing Yi (University of Texas at San Antonio)*
- A Workload-Aware Mapping Approach For Data-Parallel Programs**  
*Dominik Grewe, Zheng Wang, Michael O'Boyle (University of Edinburgh)*
- Runtime Parallelization of Legacy Code on a Transactional Memory System**  
*Matthew DeVuyst, Dean Tullsen (UCSD), Seon Kim (Korea University)*
- Cost-Aware Function Migration in Heterogeneous Systems**  
*Mario Kicherer, Rainer Buchty, Wolfgang Karl (Karlsruhe Institute for Technology)*
- 12:45-14:00 **Lunch**
- 14:30-16:30 **Visit to Knossos Archaeological Site**
- 16:30-18:30 **Visit to Zacharioudakis Winery**
- 19:00 **Banquet & Best Paper Award**



## Wednesday, 26 January

- 9:00-10:30 **Paper Session 5: Modeling and Analysis**
- Fast Modeling of Shared Caches in Multicore Systems**  
*David Eklov, David Black-Schaffer, Erik Hagersten (Uppsala University)*
- SWEEP: Evaluating Computer System Energy Efficiency using Synthetic Workload**  
*Kristof Du Bois, Tim Schaeps, Stijn Polfiet, Frederick Ryckbosch, Lieven Eeckhout (Ghent University)*
- Directly Characterizing Cross Core Interference Through Contention Synthesis**  
*Jason Mars, Lingjia Tang, Mary Lou Soffa (University of Virginia)*
- 10:30-11:00 **Coffee Break**
- 11:00-12:30 **Paper Session 6: Memory Hierarchies**
- Cache Equalizer: A Placement Mechanism for Chip Multiprocessor Distributed Shared Caches**  
*Mohammad Hammoud, Sangyeun Cho, Rami Melhem (University of Pittsburgh)*
- Replacement policies for shared caches on symmetric multicores : a programmer-centric point of view**  
*Pierre Michaud (INRIA)*
- NoC-Aware Cache Design for Multithreaded Execution on Tiled Chip Multiprocessors**  
*Ahmed Abousamra, Rami Melhem, Alex Jones (University of Pittsburgh)*
- 12:30-12:40 **Closing remarks**
- 12:40-14:00 **Lunch**

## WORKSHOPS AND TUTORIALS

### Saturday, 22 January

- RAPIDO'11 workshop
- CAOS'11: Second Workshop on Computer Architecture and Operating System Co-Design
- OpenCL Heterogeneous Computing Tutorial
- PEPHER workshop

### Sunday, 23 January

- WRC'11: 5th Workshop on Reconfigurable Computing
- DFR'11: 3rd Workshop on Design for Reliability
- MULTIPROG'11: 4th Workshop on Programmability Issues for Multicore Computers
- INA-OCMC'11: Workshop on Interconnection Network Architectures: On-Chip, Multi-chip
- Tutorial on ILDJIT: a compilation framework for program introspection, optimization and micro-architectural design