



Application of TM to a Novel Execution Model (DTA)

Cluster: Programming Models & OS

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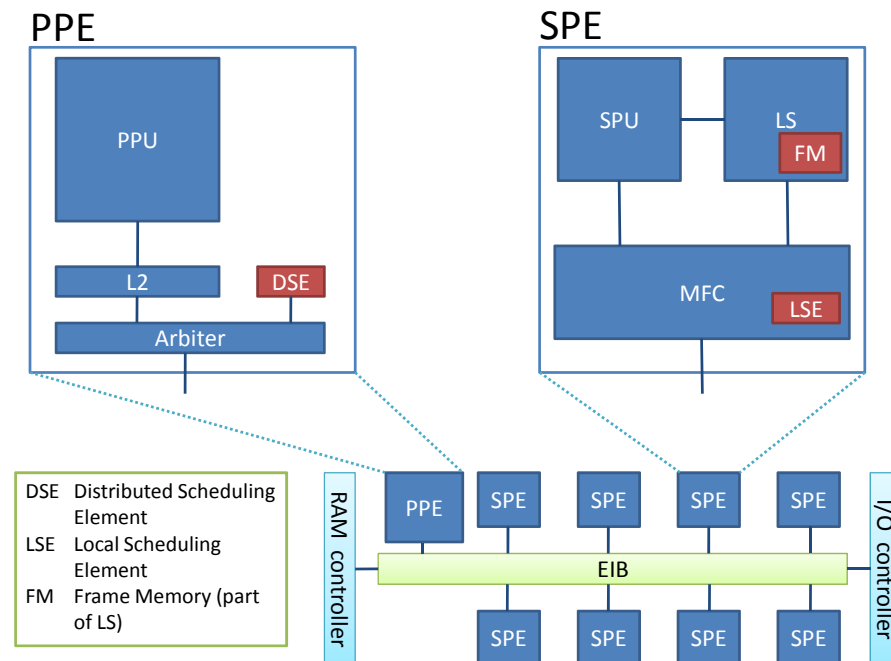
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Decoupled Threaded Architecture

- Developed in SARC (*Scalable ARChitectures*) Integrated Project

- Support for TLP and scalable HW scheduling

- Implementation of DTA in UNISIM
 - Based on Cell processor model
 - CellSim/SARCSim
 - Kept SPU ISA with DTA-specific additions



Decoupled Threaded Architecture (2)

- *Decoupled Threaded Architecture (DTA)*
 - Based on SDF, adapted for scalable multicore systems [Giorgi07a]
 - Resources divided into clusters: addressing wire-delay
 - Scalable HW Scheduling
 - Memory Access Decoupling
 - Intend to implement decoupling based on preloading data and cache locking mechanisms. [Giorgi07c]
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Application of TM to a Novel Execution Model (DTA)

- Is TM more efficient in TLP-oriented Architectures ?
 - GHC (compiler) already provides a software TM implementation
 - SARC (FP6-IP) is providing a TLP infrastructure (DTA) in UNISIM (simulator)
 - HIPEAC-1 cluster (UPC+SIENA) is implementing GCH-IR (“core”) to DTA mapping

 - Direction of collaboration/investigation:
 - Find reasonable tradeoff between HW and SW support
 - Synchronize among threads using coarse-grained dataflow
 - Overhead reduction through read/write set prediction
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References

- [Kavi01a] K. M. Kavi, R. Giorgi, J. Arul, "Scheduled Dataflow: Execution Paradigm, Architecture, and Performance Evaluation", *IEEE Trans. Computers*, ISSN:0018-9340, Los Alamitos, CA, USA, vol. 50, no. 8, Aug. 2001, pp. 834-846, doi [10.1109/12.947003](https://doi.org/10.1109/12.947003).
- [Giorgi07a] R. Giorgi, Z. Popovic, N. Puzovic, "DTA-C: A Decoupled multi-Threaded Architecture for CMP Systems", *Proc. IEEE SBAC-PAD*, ISBN:0-7695-23014-1, Gramado, Brasil, Oct. 2007, pp. 263-270
- [Giorgi07c] Giorgi R., Popovic Z., Puzovic N., "Memory access decoupling in a multithreaded architecture", (First Italian Workshop on Real Time Embedded Systems) *WIRTES 2007*, Pisa, July 2007
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