Call for Papers

5th HiPEAC Industrial Workshop
Tools and Methodology for Parallel Programming

June 4^{th}, 2008
Organized by: HP Labs, Exascale Computing Lab, Barcelona Research Office
Hewlett-Packard, Sant Cugat del Vallés, Barcelona, Spain

http://www.hipeac.net/industry_workshop5

We live exciting times in the field of parallel architectures. The diminishing IPC returns caused by power and frequency walls have forced a radical change in CPU design. Multicore is here to stay and has become pervasive throughout the computer industry. In high-performance computing, three out of four "TOP 500" systems are clusters of industry-standard multicore nodes. In embedded computing, heterogeneous multicore System-on-Chips have become the dominant standard for high-volume parts.

There is no silver bullet in multicore programming, and formidable computer science problems underlie the programming of this new breed of parallel architectures. Traditional parallel programming paradigms and tools need to be put to the test and questioned. The heterogeneity of cores and accelerators is creating new challenges to the programming models. Locks and multithreading memory semantics are being redefined and transactional programming is on the horizon. With new programming paradigms and a shifting architecture target, new tools and analysis methodologies are also granted.

The goal of this workshop is to bring together researchers from academia and industry to discuss **tools and methodologies for analysis, compilation, debugging, verification and simulation of parallel programs**.

The topics of interest include, but are not limited to:

- Compiler support for explicit parallelism (threads, transactions)
- Tools to aid programmers to identify, exploit, verify, debug, and tune parallel applications
- Simulation methodology and tools for multicore/manycore/clustered parallelism
- Characterization of parallel applications and their scalability
- Reliability and Fault Tolerance for applications running on many-core and distributed architectures
- I/O issues in parallel computing and parallel applications
- Parallel programming languages, algorithms and applications
- Middleware and run time support for parallelism

Important Dates

Submission deadline	April 25^{th}, 2008
Notification of acceptance	May 2^{nd}, 2008
Workshop	June 4^{th}, 2008

Submissions

Authors should submit their contributions electronically to Daniel Ortega (hipeac.workshop@hp.com). Submissions must include a 2-page extended abstract describing the work that is going to be presented. Authors should feel free to present work in progress as well as already published material, and can include related documents with additional details on their research work. Authors should commit to present their research at the workshop in the case it gets selected. Abstract and other workshop material will be made available online at http://www.hipeac.net/. The workshop will not publish proceedings. While this workshop is organized by HiPEAC, the host (HP Labs) is solely responsible for the selection process.

Feel free to forward this call for papers in your institution.