HiPEAC^2: 5th Meeting of the Task Force on Reliability and Availability

Wroclaw, October 27, 2009

Munich Agenda

- Overview of TF - 5min
- Discussion about the aims of the TF and how to achieve them – 15min
- Technical Presentations - 50min
  - Oguz Ergin, TOBB University
  - Stelios Mamagkakis, IMEC

- Time Permitting:
  - Operation below Vcc-min
  - DRAM Failures: Case study on Google Servers

Reliability and Availability

Technology developments are presenting us with the challenge of building computer systems made of unreliable parts.

Worst scenario: reliability constraints may obviate the benefits of technology scaling. High cost to provide reliability and availability slows down ICT and economic growth.

Future systems need to be Dependable: ability to operate correctly and satisfactory in the presence of faults

- Online detect, correct, diagnosis, repair
- Reduced down time
- High dependability/euro ratio

HiPEAC's response

Task Force on reliability and availability to promote awareness and research in this area

Orthogonal to many clusters

Instruments

- Regular meetings in the HiPEAC cluster context
- Exposure to industrial perspective
- Awareness about activities in different groups
- Who is who: key players, conferences, workshops
- Tutorials, workshops, conference, summer school courses
- Project proposals
- Contribute to the roadmap
- Other?

Activities

Meetings

- 1st Barcelona, 6.2008
- 2nd Paris 11.2008
- 3rd Paphos 1.2009
- 4th Munich 6.2009

Presentations (academic and industrial)

Define R&A problem/implications/solutions

Discussions about what reliability means

Workshops with Micro41 and HiPEAC09

Tutorial with HiPEAC09

Contribute in the roadmap

FP7 proposals

Todos

Suggestions of issues you like see discussed/ addressed. How?
Role of the task force? yanos@cs.ucy.ac.cy

Todos/Suggestions

1. Register in the R&A TF email list
2. Send me email with brief description of your research activity and link to your project web site
3. Check TF web page. suggestions for other info to include,
   - Improve web page presentation, links from our web-pages
   - Make web page focal point/increase visibility
4. Participate and contribute in future meetings and R&A TF related events
5. Increase R&A awareness in the other clusters

NEWS

2nd Workshop on Design for Reliability in conjunction with HiPEAC 2010.

- Deadline for submitting papers Nov. 1st

IEEE TC Special Issue on Dependable Computer Architecture

- Deadline Jan. 15, 2010

Mini-sabbaticals opportunity for up to 3-month visits to industry or other institutions

Munich Agenda

- Overview of TF
- Discussion about the aims of the TF and how to achieve them
- Technical Presentations
  - Oguz Ergin, TOBB University
  - Stelios Mamagkakis, IMEC
- Short Intro to Eurocloud (FP7 Strep Project)

- Time Permitting:
  - Operation below Vcc-min
  - DRAM Failures: Case study on Google Servers

Operation Below Vcc-min

Address process-variability

Eliminate voltage margins, operate at voltage level where certain fraction of transistors may become unreliable

Trade-off performance(cache capacity) for power

Rely on run-time tests to determine faulty cells

Discussion:

- What happens to the combinational logic?
- Bigger transistors, variable latency units, voltage interpolation, …
- Multiple voltage domains?

Wilkerson et al. ISCA08, session MICRO09

DRAM Errors Case Study on Google servers

Study of many different types of servers over a 2.5 yr period

3 type of systems use memory scrubbers, 1GB/45min

8% of DIMMs affected by errors/year

- Most of them correctable (0.22% of DIMMs observe uncorrectable errors)- ECC helps by factor of 40

Error correlation (errors more likely to occur on dimm that experiences faults)

- Errors not dominated by soft-errors

Uncorrectable is usually preceded by correctable error (however, difficult to predict time-delta)

Aging clearly affects observed errors (exponential growth)

Schroeder et al. Sigmetrics09

Thank you for participating!

See you in Pisa!