

SELSE

IEEE workshop on Silicon Errors in Logic and System Effects

Papers from academia and industry

Several papers reported on measurements and analysis of soft-errors when chips are exposed to neutron beams

Consider SE for memory array cells, flops in non-arrays and logic

There is a consensus that 10% design overhead for reliability “acceptable”

Desirable to have predictability and determinism (today)

SELSE

AVF

what resources are most critical to protect

input affects AVF

Predictive models based regression based analysis can be used to predict AVF on the fly

Introduce code assertions to detect invariant violations (e.g. a function that returns either a 1 or 0)