

Rapid Performance Evaluation of MPSoC Platforms

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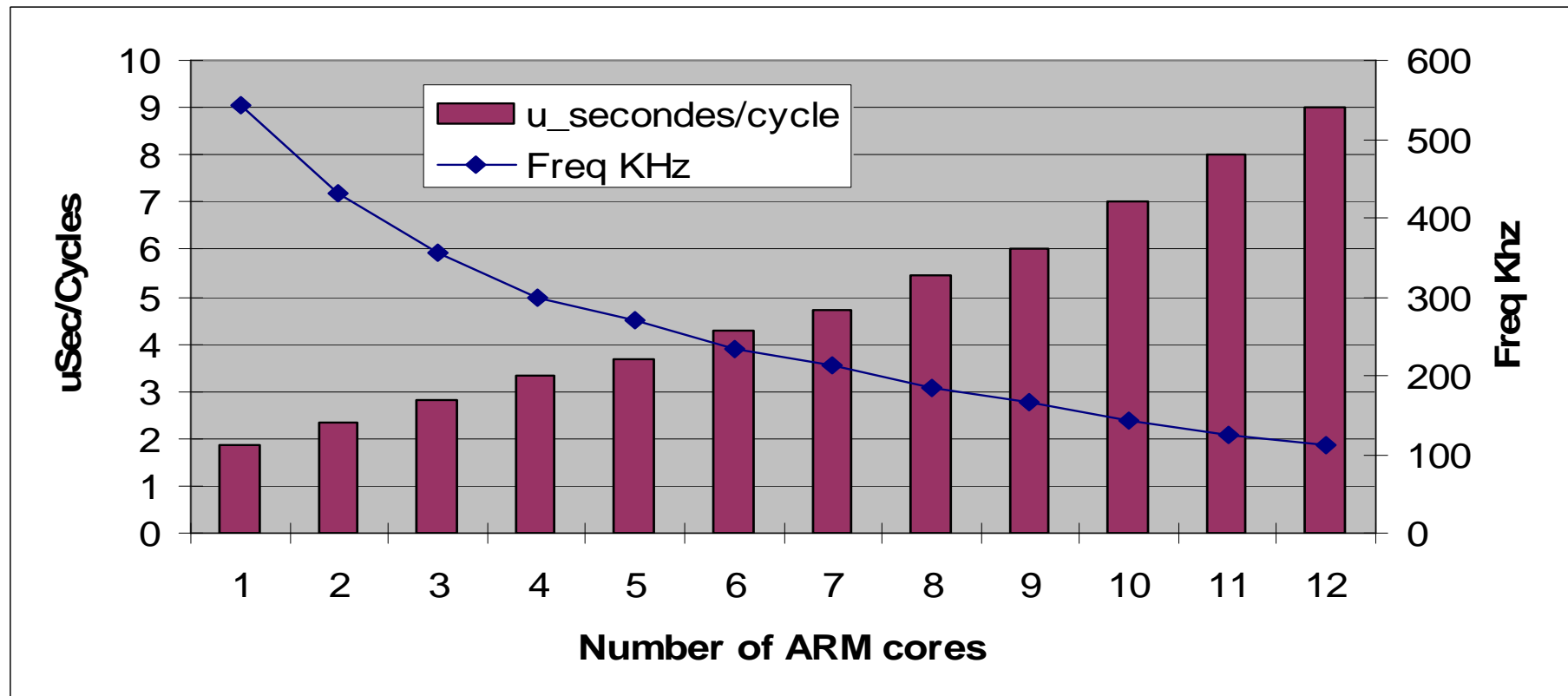
- ✓ Simulation for embedded systems vital position (Time-to-market)
- ✓ Design space configuration (DSE):
 - ☞ Find the best MPSoC configuration
- ✓ But with ↑ complexity circuit (VLSI): conventional "cycle/bit accurate" tools problematic.
 - ☞ increase in simulation time:
 - 1sec on the real system : several hours of simulation

- Aim: explore the maximum # alternatives in reduced time interval.
- 2 issues:
 - Reducing the number of alternatives to explore: meta-heuristics (Taboo search, GA, ..etc)
 - Reducing the time associated with configuration evaluation (fitness calculation)

Why simulation acceleration for MPSoC is important??



Rijndael on an MPSoC platform



u_sec/sycle: time in u-sec for simulating 1 cycle of the MPSoC

Freq: the number of simulated MPSoC cycles /sec

Simulation time (u_sec for 1 cycle) increases with # cores

Simulation Acceleration Methods

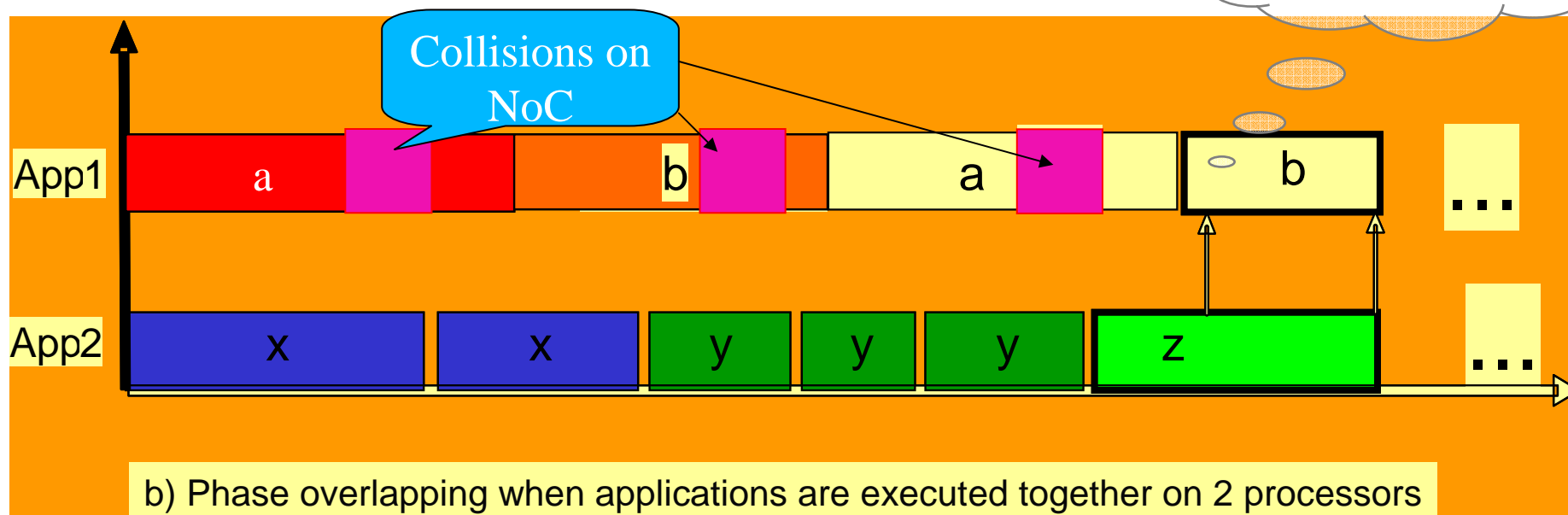
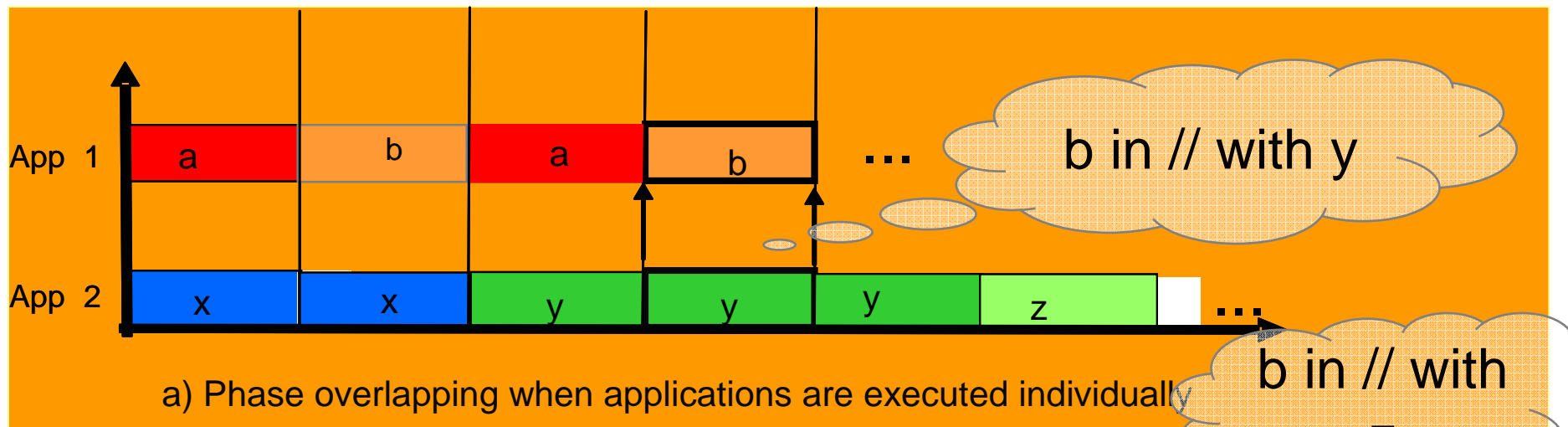


1. **Statistical Simulation***: Generate a "Synthetic program" with smaller number of instruction but same profile (architectural behavior).
2. **Analytical Modeling***: Performance/power consump. is approximate analytically (math. models).
3. **Higher level models**: architectural details are hidden, "Transactional Level Modeling" TLM.
4. **Sampling****:
 - 1 or several samples (or intervals) of the appli. are chosen.
 - Samples: smaller instruction count, represent the whole appli. behavior.

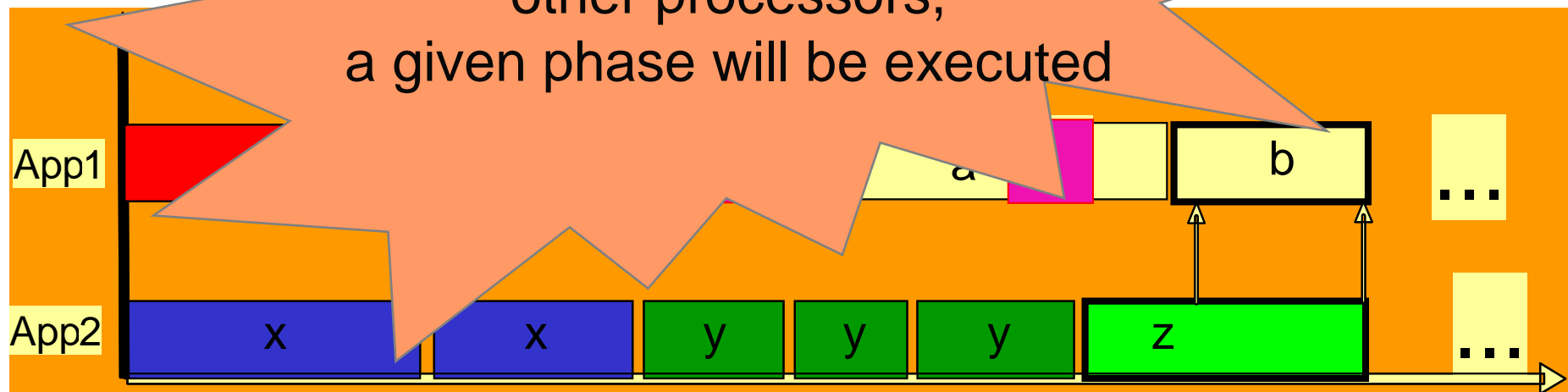
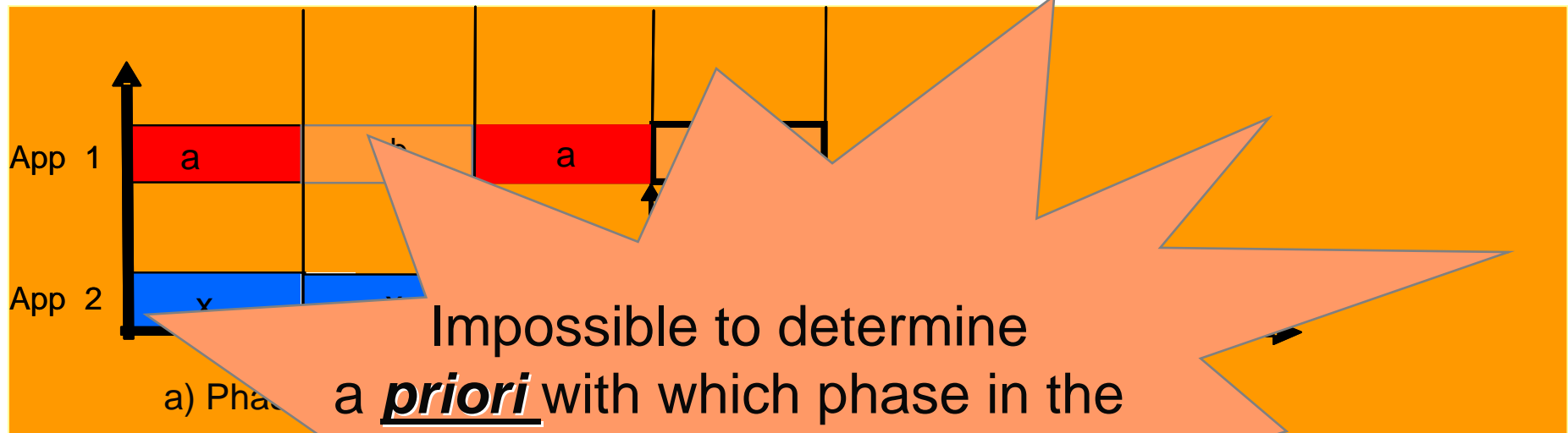
*in collaboration with L.Eeckhout and K.De Bosschere(ELIS, U.Ghent)

** in collaboration with K.Z.Ibrahim, Univ. of Port Said, Egypt

Sampling for Multiprocessors not Obvious!!!



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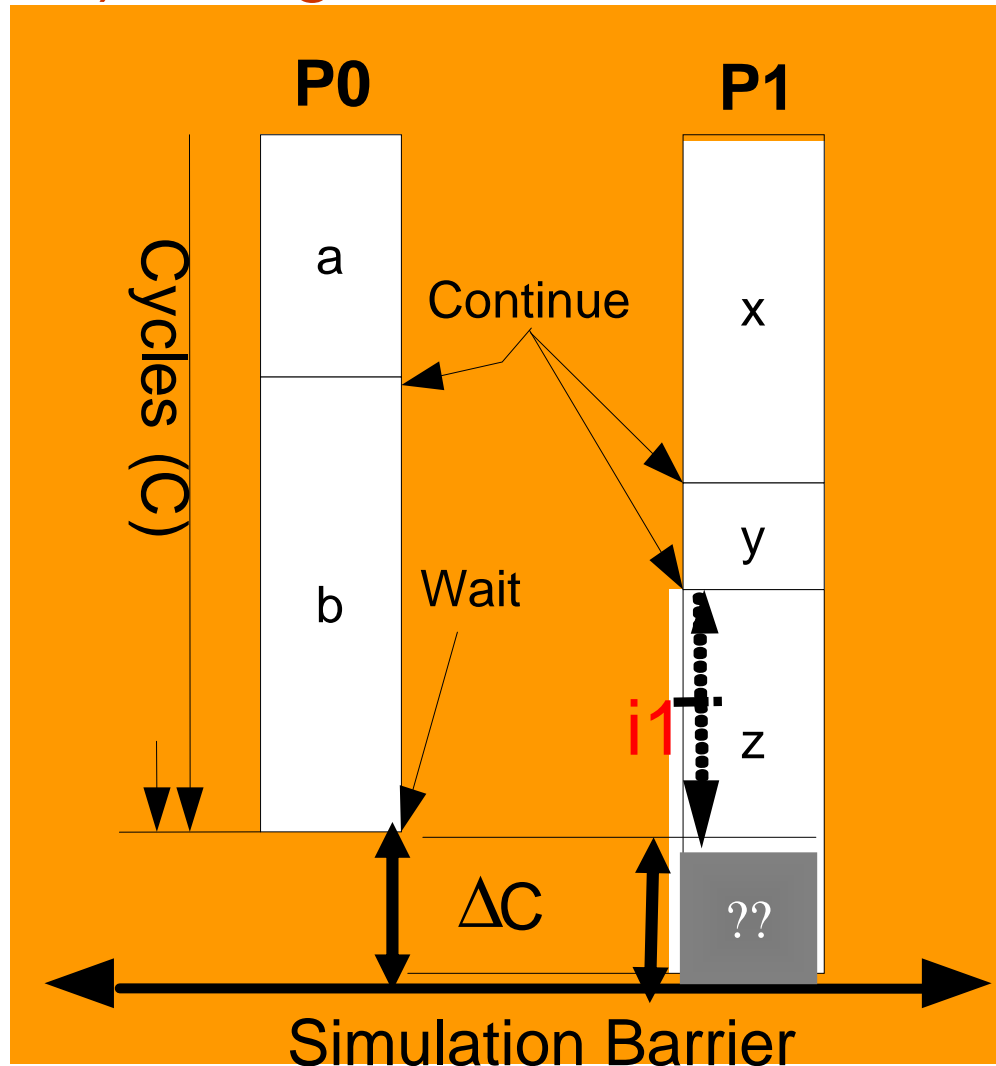


- **First Step** : *program tracing and phase identification*
 - Phase-ID trace for each processor.
 - Obtained traces are independent other // processors & MPSoC architectural configuration.
 - Accomplished once for all the configurations
 - Rapid functional simulation is used

In a few minutes, a processor phase trace is obtained

Interval (in K Inst)	P0 phases	P1 phases
0-50	a	x
50-100	b	y
100-150	c	z
150-200	d	w
200-250	a	x
250-300	b	y
350-400	f	z

A) Using simulation barriers for CS generation



P0
 $\Delta C =$ estimated nbr of cycles to terminate z in P1

if $\Delta C < \text{Threshold (TWSB)}$:
 • Generate Syn. barrier

Else : continue simulation

b) Using CST for simulation acceleration



Phase ID Traces

Number of Instructions (*1000)	Phase ID Traces	
	P0 phases	P1 phases
0-50	a	x
50-100	b	y
100-150	c	z
150-200	d	w
200-250	a	x
250-300	b	y
350-400	f	z

Cluster of Strings CS

Simulation Barriers

Not Simulated

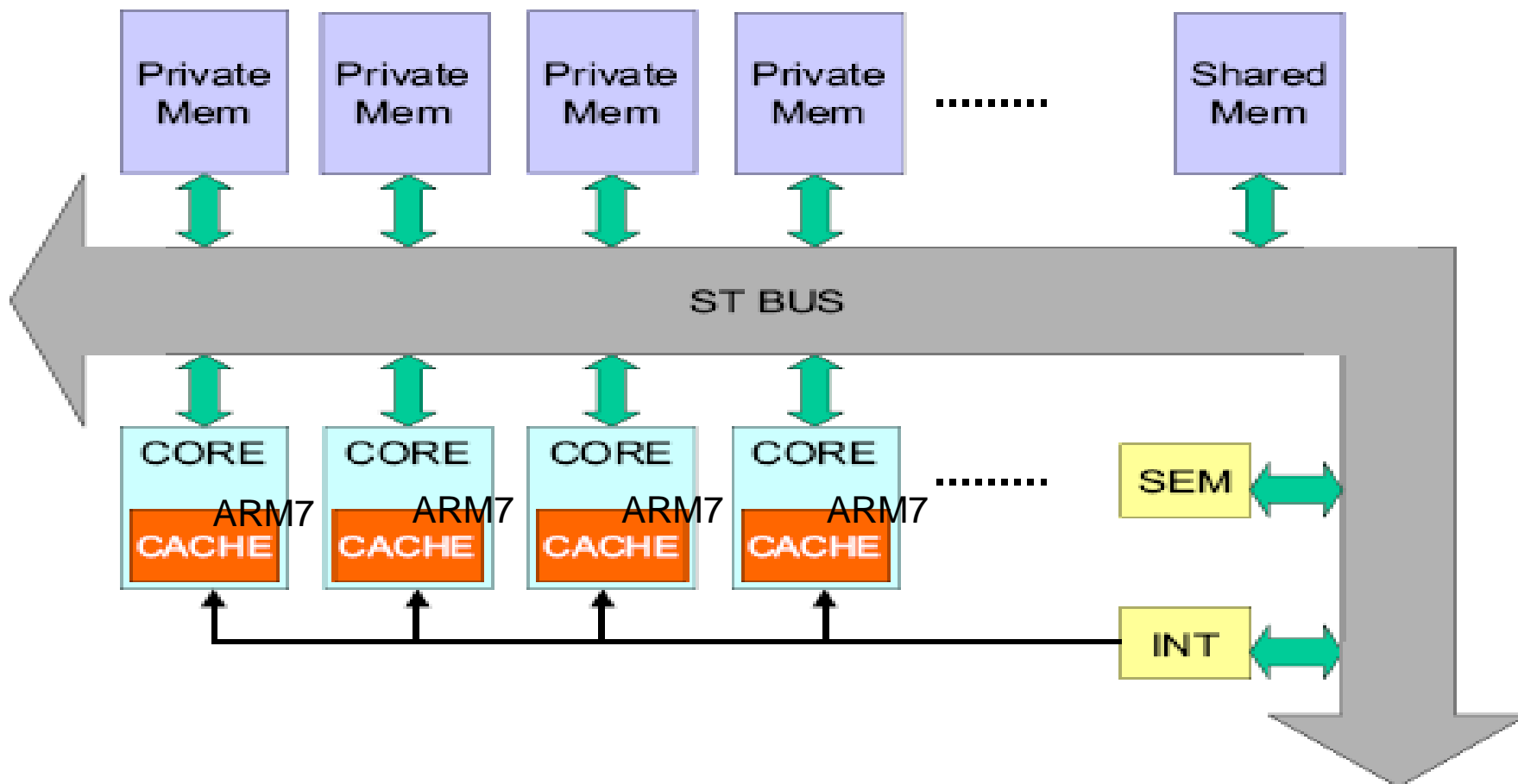
Cluster String Table (CST)

Cluster	Inst. Count P0 (K)	Inst. Count P1 (K)	Cycles	Energy	Repetition
a,b - x,y,z	100	150	C1	E1	2
c,d - w	100	50	C2	E1	1



1. **First step:** generate application individual phase-ID trace (PIDT) file
2. **Second Step:** For each CS in CST, determine if it corresponds to the next set of strings in PIDT's
 - If match, skip detailed simul. up to the next synchro. barrier.
 - Else
 - a) Detailed simulation is performed.
 - b) At the end of 1 simulated interval by a core:
 - If remaining cycles for all processors $<$ threshold?
 - i. All cores stop sim. at end of current intervals
 - ii. A new entry the CST, record CS performances in CST.
 - Else:
Go to 2, unless PIDTs empty

Platform : MPARM, ARM 7 (up to 12 core), SystemC, Intercommun. D&I\$ 8KB.

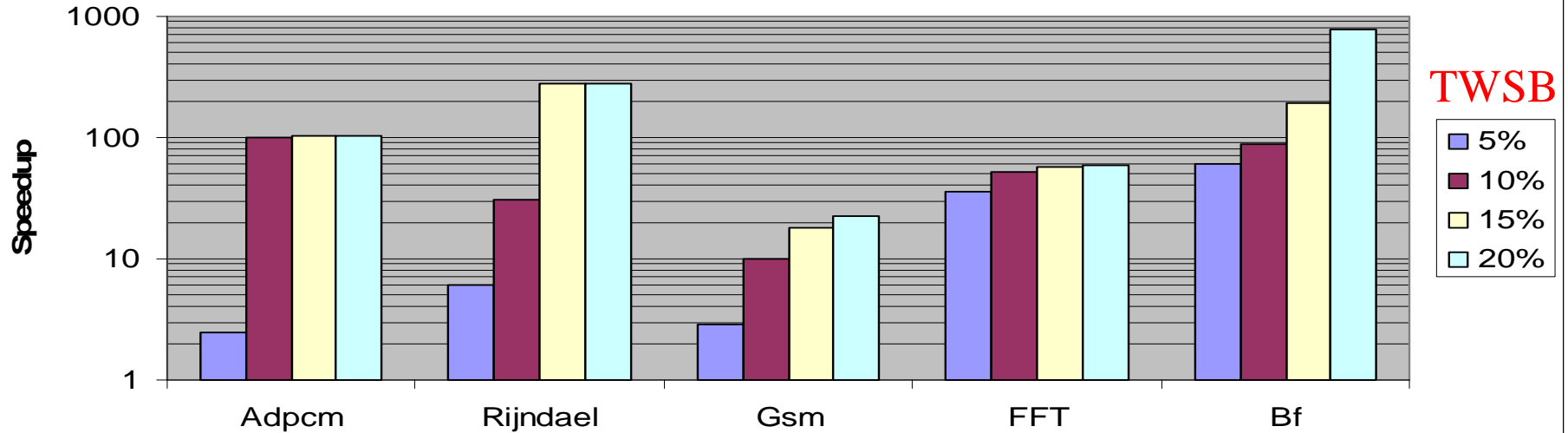




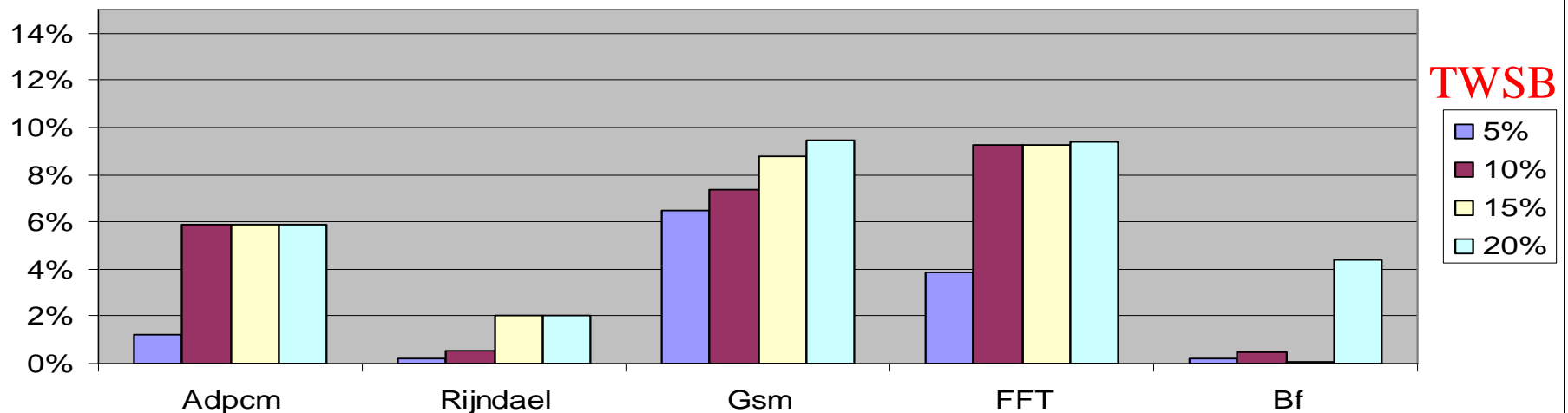
Acceleration and error



SpeedUp for different TWSB with 4 processors



Error for different TWSB with 4 processors



1. Automatic setting of the threshold (TWSB)
 - ◆ Desired speedup set by the user.
 - ◆ Provide the smallest possible estimation error.
2. More complex processor and network architectures will be integrated into the platform.
3. Checkpointing btw simulated clusters
4. Hybrid simulation
 - ◆ The number and the category of alternatives must be chosen fct of the simulation level/technique (CABA, Sampling, TLM, FPGA)

- ***Rapid Performance and Power Consumption Estimation Methods for Embedded System Design***, Workshop on Rapid System Prototyping RSP'06.
- ***An MPSoC Performance Estimation Framework Using Transaction Level Modeling***. Conference on Embedded and Real-Time Computing Systems and Applications, RTCSA'07.
- ***Adaptive Sampling for Efficient MPSoC Architecture Simulation***. Symposium on Modeling, Analysis, and Simulation of Computer and Telecommunication Systems (MASCOTS'07).