

Nanoc

- Nanoscale silicon-aware network-on-chip design platform
- Frank Olaf Sem-Jacobsen

Simula Research Laboratory AS

- **October 19, 2010**



Scope

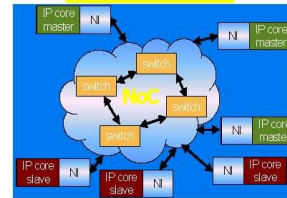
- The NaNoC consortium was set up in response to Challenge 3 (Components, Systems, Engineering), Objective ICT-2009.3.2: Design of Semiconductor Components and Electronic Based Miniaturised Systems.
- Target outcome: ***improved design platforms, interfaces, methods and tools that meet the requirements of semiconductor companies, fab-less design houses and system developers***

- **The gap**

- There is no concise way of communicating all architectural issues down to the physical layer
- Similarly, there is no concise way of communicating all physical issues up to the architectural layer

System management frameworks

ARCHITECTURAL GAP
Virtualization, dynamism in NoC component assembly, DVFS



PHYSICAL GAP
Building reliable components out of unreliable devices and uncertain technology parameters

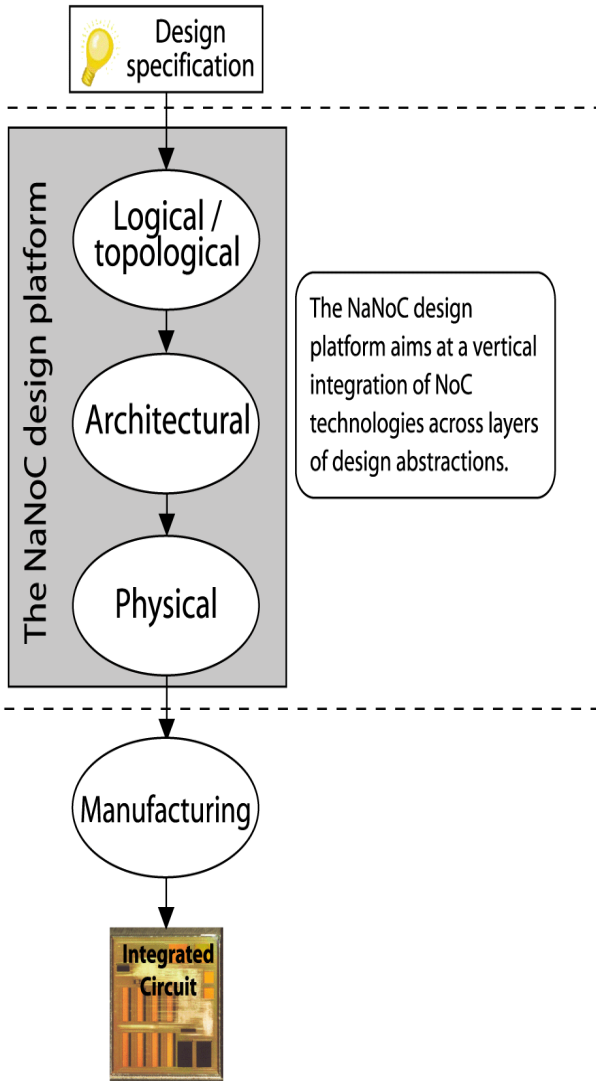
Intricacies of nanoscale design

Design technology of current NoCs is not suitable for future requirements

Need for a new NoC design platform

Design methods of current NoCs are not suitable for future requirements

Design challenges that are not met by current methods



- **Defects** Both fabrication failures and progressive wear-out over time
- **Heterogeneity** Future SoCs will consist of a multitude of different systems, in both regular and irregular patterns
- **Virtualisation** This is required to support manageability, reliability, security and mapping as outlined in the roadmap of many semiconductor companies
- **Cross-layer design** A choice made in any design layer (from architecture down to physical layout and timing) may have unforeseen side-effects in other layers

The consortium



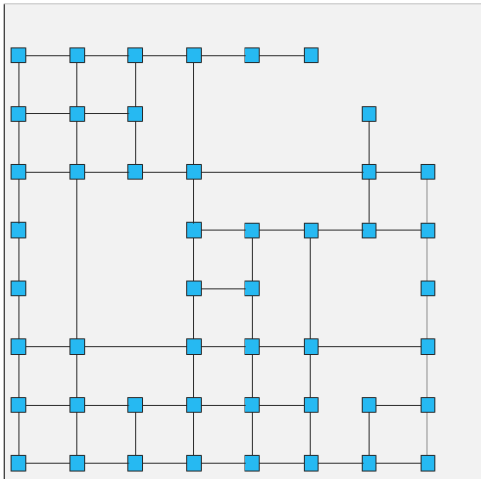
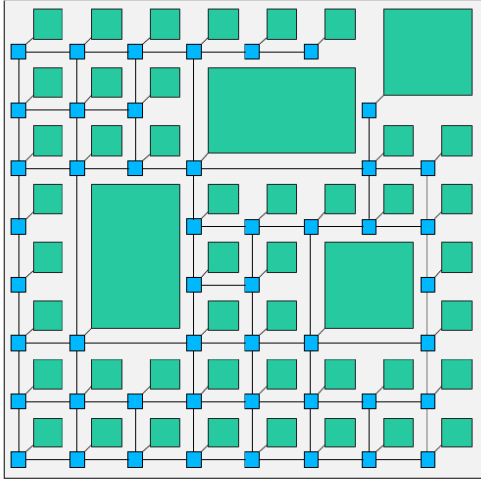
[**simula** . research laboratory]
- *by thinking constantly about it*



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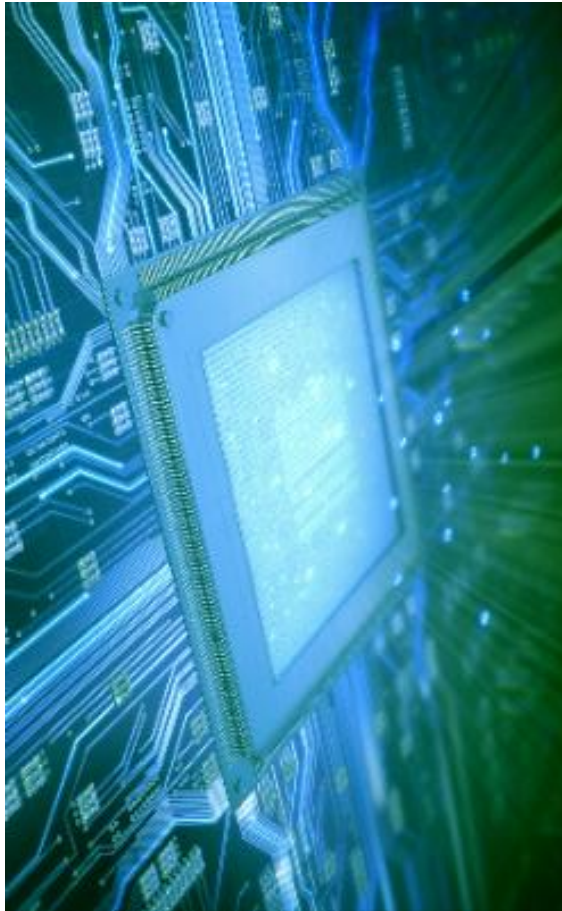
- The partners cover the spectrum of the full design space
 - Network architecture
 - Network component design
 - Topology synthesis
 - Floor planning
 - Chip design
- Start date: January 1, 2010
 - To December 31, 2012

Support for static and dynamic irregularities



- Topology agnostic logic-based routing
 - CMP
 - LBDR, FDOR
 - Application-specific
- Multicast, cache coherency
- Reconfiguration
- Quality of service
- Task allocation/virtualisation
- Topology generation
- Methods to detect and combat process variability

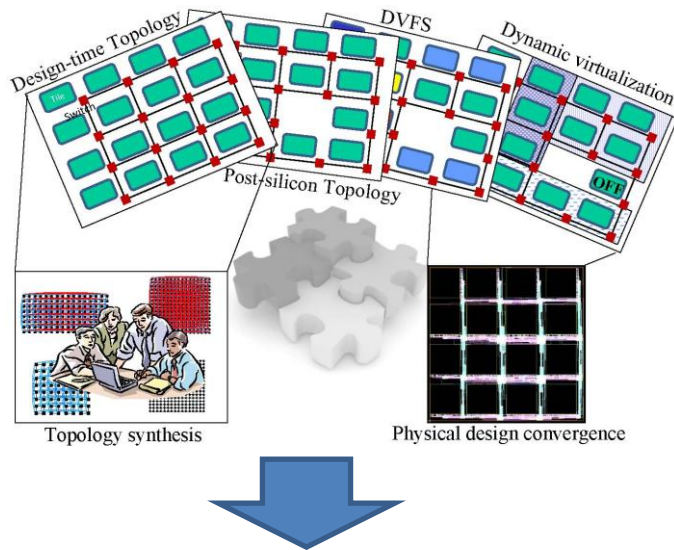
Hardware interoperability



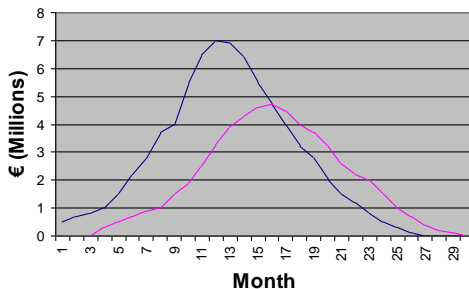
http://www.low-powerdesign.com/article_silistix_lautzenheiser.htm

- NoC support for standard IP libraries
- 3-D stacking
- Timing robustness
- Power grid and variability modelling
- Designing and testing the NaNoC switch

Communication Exchange Format



Revenue for two companies



- CEF is the glue that binds the toolchain together
 - Allows for bidirectional information flow
 - Improves the efficiency of multiple design iterations

Publications

- www.nanoc-project.eu



http://www.fromoldbooks.org/pictures-of-old-books/pages/img_7378-stack-of-books/

Process Variation and Layout Mismatch Tolerant Design of Source Synchronous Links for GALS NoC

A. Strano, D. Bertozzi, C. Hernández, and F. Silla
12th IEEE International Symposium on System-on-Chip (SoC 2010)
Tampere, Finland, September 28-30, 2010
ISBN: 978-1-4244-8276-4
Pages: 43-48

A methodology for the characterization of process variation in NoC links

C. Hernandez, F. Silla, J. Duato
Design, Automation & Test in Europe Conference & Exhibition (DATE), 2010, (2010)

Improving the Performance of GALS-based NoCs in the Presence of Process Variation

C. Hernandez, A. Roca, F. Silla, J. Flich, and J. Duato
4th ACM/IEEE International Symposium on Networks-on-Chip (NOCS 2010)
Grenoble, France, May 3rd-6th, 2010
ISBN: 978-0-7695-4053-5
pages: 35-42

Addressing Manufacturing Challenges with Cost-Efficient Fault Tolerant Routing

Samuel Rodrigo, José Flich, Antonio Roca, Simone Medardoni, Davide Bertozzi, Jesús Camacho, Federico Silla and José Duato
Best Paper Award
4th ACM/IEEE International Symposium on Networks-on-Chip (NOCS 2010)
Grenoble, France, May 3rd-6th, 2010
ISBN: 978-0-7695-4053-5
Pages: 25-32

Improved Utilization of NoC Channel Bandwidth by Switch Replication for Cost-Effective Multi-Processor Systems-on-Chip

Francisco Gilbert, María Engracia Gómez, Simone Medardoni and Davide Bertozzi
4th ACM/IEEE International Symposium on Networks-on-Chip (NOCS 2010)
Grenoble, France, May 3rd-6th, 2010
ISBN: 978-0-7695-4053-5
Pages: 165-172