



# CALL FOR PAPERS

## HiPEAC 2010

### 2010 International Conference on High-Performance Embedded Architectures and Compilers

January 25-27, 2010  
Pisa, Italy

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The challenges faced by the high-performance general-purpose and embedded worlds are converging. The embedded market evolves rapidly, quickly expanding the capabilities of new devices, and the requirements of these new applications demand technologies that not long ago were in the realm of high-performance computing. Conversely, the energy and cost constraints typical of the embedded world are now also among the most important design criteria for general purpose computing systems. Because performance no longer automatically increases with advances in semiconductor technology, it has become essential to discover new paths to optimize performance, energy and cost across software and hardware.

The HiPEAC conference provides a forum for computer and compiler architects in the field of high performance architecture and compilation for embedded and general-purpose systems, with a special emphasis on cross-cutting research that can be applied to both. The conference aims at the dissemination of advanced scientific knowledge and the promotion of international contacts among scientists from academia and industry. Topics of interest include, but are not limited to:

- Processor architecture and instruction-level parallelism
- Multi- and many-core architectures (e.g., homogeneous, heterogeneous MPSoC)
- Memory system design and optimization
- Power, performance and cost efficient processor designs
- Domain specific architectures (e.g., Network, Security or Graphics processors)
- Application specific architectures, ASIPs, accelerators, customized processors
- Reconfigurable architectures and tools for reconfigurable computing
- Compilation techniques for embedded processors
- Dynamic, adaptive and continuous optimization and compilation
- Back-end code generation and scheduling
- Binary translation and optimization
- Compilation and runtime support for multi- and many-core architectures
- Tools and techniques for simulation and performance analysis
- Program and workload characterization and profiling techniques
- Tools for analysis, design, testing and implementation of embedded systems

Submit an electronic copy of your paper (in PDF) not exceeding 16 pages and 5,000 words, following the instructions at <http://www.hipeac.net/conference> by **July 3, 2009**.

HiPEAC also welcomes half-day tutorial and workshop proposals. They should be submitted directly to the workshops/tutorials chair by **June 16, 2009** and notification will be given by June 26.

#### IMPORTANT DATES

- **Abstract due:** July 3 (11.59 PM, PDT), 2009
- **Paper due:** July 10 (11.59 PM, PDT), 2009
- **Notification:** Sept 15, 2009
- **Final paper due:** October 30, 2009