



# DSD2009

## 12<sup>th</sup> EUROMICRO CONFERENCE on DIGITAL SYSTEM DESIGN Architectures, Methods and Tools

# Call for Papers

Patras, Greece. 27-29 August 2009

### CONFERENCE COMMITTEE

#### DSD STEERING COMMITTEE:

Chairman: Lech Józwiak, Eindhoven Univ. of Tech. (NL)  
Krzysztof Kuchcinski, Lund Univ. (SE)  
Antonio Nunez, IUMA/Univ. of Las Palmas GC (ES)

#### DSD09 GENERAL CHAIRMAN:

Odysseas Koufopavlou, Univ. Patras (GR)

#### DSD09 PROGRAM COMMITTEE CHAIR:

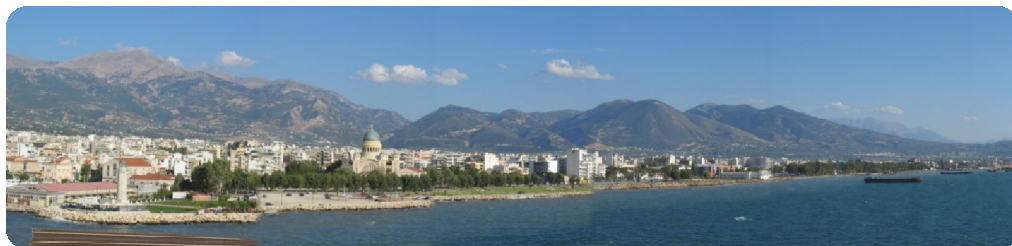
Program Chairman:  
Antonio Nunez, IUMA/Univ. of Las Palmas GC (ES)  
Deputy Program Chairman:  
Pedro P. Carballo, IUMA/Univ. of Las Palmas GC (ES)

#### DSD09 LOCAL ORGANIZING CHAIR:

Chair: Paris Kitsos, HOU Hellenic Open Univ. (GR)  
Co-chair: Henry Basson, Univ. of Littoral (FR)  
Co-chair: Nicolas Sklavos, TEI Patras (GR)

#### DSD09 PROGRAM COMMITTEE:

A. Akkas, Koc Univ. (TK)  
L. Benini, Univ. of Bologna (IT)  
M. Biglari-Abhari, Univ. of Auckland (NZ)  
P. P. Carballo, Univ. of Las Palmas GC (ES)  
S.J. Chen, National Taiwan Univ. (TW)  
C. Cornelius, Rostock Univ. (DE)  
M. Danek, UTIA (CZ)  
G. Danese, Univ. Of Pavia (IT)  
J.L. Dekeyser, Univ. of Lille (FR)  
R. Drechtler, Univ. of Bremen (DE)  
N. Dutt, Univ. of California, Irvine (US)  
P. Eles, Linköping Univ. (SE)  
L. Fanucci, Univ. of Pisa (IT)  
M. Figueroa, Univ. of Concepcion (CL)  
L. Józwiak, Eindhoven Univ. of Tech. (NL)  
K. Judmann, Tech. Univ. of Vienna (AT)  
B. Juurlink, TU Delft (NL)  
K. Kent, Univ. Brunswick (CAN)  
P. Kitsos, HOU Patras (GR)  
Z. Kotasek, Brno Univ. of Tech. (CZ)  
O. Koufopavlou, Univ. of Patras (GR)  
H. Kubatova, CTU in Prague (CZ)  
K. Kuchcinski, Lund Univ. (SE)  
S. Kumar, Jonkoping Univ. (SE)  
M. Kuwahara, Toshiba Corp. (JP)  
F. Leporati, Univ. of Pavia (IT)  
T. Luba, Warsaw Univ. of Tech. (PL)  
H. Maehle, Univ. of Luebeck (DE)  
E. Martins, Univ. of Aveiro (PT)  
J.S. Matos, Univ. of Porto (PT)  
V. Muthukumar, UNLV (US)  
N. Nedjah, State Univ. of Rio de Janeiro (BR)  
S. Niar, Univ. of Valenciennes (FR)  
S. Nooshabadi, Gwangju Inst. of Sc&Tech (KR)  
A. Nunez, Univ. of Las Palmas GC (ES)  
A. Orailoglu, UC, San Diego (US)  
A. Pawlak, SUT (PL)  
M. Perkowski, Portland St. Univ. (US)  
A. Postula, Univ. of Queensland (AU)  
J. Rabaey, Univ. of California, Berkeley (US)  
B. Rouzeyre, Univ. of Montpellier II (FR)  
S. Ruelke, IIS-FhG Dresden (DE)  
T. Sasao, Kyushu Inst. of Tech. (JP)  
A. Shrivastava, Univ. of Arizona (US)  
J. Tiberghien, VUB Free Univ. of Brussels (BE)  
D. Timmerman, Rostock Univ. (DE)  
R. Ubar, Tallinn Tech. Univ. (EE)  
M. Valero, Pol. Univ. of Catalunya (ES)  
M. Velev, Consultant (US)  
H.T. Vierhaus, Brandenburg Univ. of Tech. (DE)  
S. Vitabile, Univ. of Palermo (IT)  
C. Wolinski, IRISA, Rennes (FR)  
A. Zemva, Univ. of Ljubljana (SI)



### SCOPE

The Euromicro Conference on Digital System Design (DSD) addresses all aspects of digital system design from embedded and mixed hardware/software system engineering, down to microarchitectures, digital circuits and VLSI techniques. It focuses on advanced circuit and system design and design automation concepts, paradigms, methods and tools, as well as on modern implementation technologies from full custom in nanometer technology nodes to FPGA and to multicore infrastructures. Compiler assisted ASIP, CMP, SMP, SMT, DSP-VLIW, GPU and platform based system design research results are welcome. Design and Verification Languages and Standards, Modeling, High Level Synthesis, Productive Design Technology and Engineering Flows, Efficiency, Density, Signal Integrity, Testability, Timing Analysis and Timing Closure, Power Consumption, Computational Power Speed and Performance, Manufacturability, Cost, Reliability, Error Resilience, Complexity, or Process Variability issues are covered in DSD.

Euromicro was founded in 1973 by Rodney Zaks and other colleagues shortly after the announcement of the Intel 4004 landmark processor. IEEE Computer Society publishes the DSD Proceedings which are available worldwide through IEEE Xplore Digital Library.

### MAIN TOPICS

**T1: (SS) - System synthesis.** High-level, behavioral, register-transfer, logic and physical circuit synthesis; arithmetic, signal processing and vector processing units; graphics processing units and hardware accelerators; memory design; communication architecture and protocols; specific circuits and processors; multi-objective optimization observing power, performance, communication traffic, interconnect architecture, layout, technology, reliability, robustness, security, testability and other issues; management of parallel computational resources, memory allocation and hierarchy; hardware/software co-design; mapping of applications and architectures; algorithm architecture matching; transaction level modeling and higher-level modeling; virtual system prototyping; design space exploration; synthesis of asynchronous and dataflow driven systems.

**T2: (MPSoC) - Systems-on-a-chip and Multiprocessor SoCs.** Generic system platforms and platform-based design; CMP, SMP, SMT, DSP and VLIW (multi)processor architecture and enhancements; networks on chip; power, energy, timing, predictability and other quality issues; IP design, standardization and reuse; virtual components; compiler assisted ASIP and MPSoC generation and configuration; hardware support for embedded kernels; embedded software features; SoC design environments for embedded systems, sequential and parallel applications; static, run-time and dynamic optimizations of embedded systems; performance metrics.

**T3: (RC) - Programmable/re-configurable architectures.** Processor, communication, memory and software architectures with focus on application specific and/or embedded computing; systems on re-configurable chip; system FPGAs and structured ASICs and co-processors; processing arrays; programmable fabrics; novel logic block architectures, combination of FPGA fabric and system blocks (DSP, processors, memories, etc.); compiled accelerators, reconfigurable computing, adaptive computing devices, systems and software; optimization of FPGA-based cores; novel design algorithms for FPGA features; embedded software; CAD for placement, routing, retiming, logic optimization, technology mapping, system-level partitioning, logic generators, testing and verification; CAD for modeling, analysis and optimization of timing and power; high-level models and tools for FPGAs; rapid prototyping.

**T4: (SMVT) - System, hardware and embedded-software specification, modeling, verification and test.** Design and verification languages; functional, structural and parametric specification and modeling; simulation, emulation, prototyping, and testing at the system, register-transfer, logic and physical levels; co-simulation and co-verification.

**T5: (APP) - Applications of (embedded) digital systems with emphasis on demanding and new applications** in fields such as: (wireless) communication and networking; measurement and control; health-care and medicine; military, space, avionics and automotive systems; surveillance and security; networked and electronic media; multimedia design; real time signal processing hardware; digital video technology; consumer electronics; ambient intelligence; wireless sensor networks; ubiquitous, wearable and implanted systems.

**T6: (ET) - Emerging technologies, system paradigms and design methodologies.** Deep sub-micron VLSI design issues; digital design in 3D layouts; optical, bio, nano and quantum technologies and computing; self-organizing and self-adapting systems.

