



May 25 – 26, 2009

Rome, Italy

<http://www.ece.lsu.edu/vaidy/raw/>

### Call for Papers

Submission Deadline: October 31, 2008



The 16<sup>th</sup> Reconfigurable Architectures Workshop (RAW 2009) will be held in Rome, Italy in May 2009. RAW 2009 is associated with the 23<sup>rd</sup> Annual International Parallel & Distributed Processing Symposium (IPDPS 2009) and is sponsored by the IEEE Computers Society's Technical Committee on Parallel Processing. The workshop is one of the major meetings for researchers to present ideas, results, and on-going research on both theoretical and practical advances in Reconfigurable Computing.

#### Run-Time Reconfiguration & Adaptive Computing: Architectures, Algorithms, Technologies

Run-Time and Dynamic Reconfiguration are characterized by the ability of underlying hardware architectures or devices to rapidly alter (on the fly) the functionalities of its components and the interconnection between them to suit the problem. Key to this ability is reconfiguration handling and speed. Though theoretical models and algorithms for them have established reconfiguration as a very powerful computing paradigm, practical considerations make these models difficult to realize. On the other hand, commercially available devices (such as FPGAs and new coarse-/multi-grain devices) appear to have more room for exploiting run-time reconfiguration (RTR). An appropriate mix of the theoretical foundations of dynamic reconfiguration, and practical considerations, including architectures, technologies and tools supporting RTR is essential to fully reveal and exploit the possibilities created by this powerful computing paradigm. RAW 2009 aims to provide a forum for creative and productive interaction between all these disciplines.

#### Topics of Interest

Authors are invited to submit manuscripts of original unpublished research in all areas of dynamic and run-time reconfiguration (foundations, algorithms, hardware architectures, devices, systems-on-chip (SoC), technologies, software tools, and applications).

Papers targeting entire applications and systems rather than isolated kernel implementations are especially encouraged. The topics of interest include, but are not limited to:

<b>Models &amp; Architectures</b>	<b>Algorithms &amp; Applications</b>	<b>Design, Technologies &amp; Tools</b>
<ul style="list-style-type: none"> <li>• Interconnect and Computation Models</li> <li>• RTR Models and Systems</li> <li>• RTR Hardware Architectures</li> <li>• Simulation and Prototyping</li> <li>• Bounds and Complexity Issues</li> <li>• Heterogeneous Computing Platforms</li> <li>• Fault Tolerant Computing</li> <li>• High Performance Computing</li> </ul>	<ul style="list-style-type: none"> <li>• Algorithmic Techniques</li> <li>• Mapping Parallel Algorithms</li> <li>• Distributed Systems &amp; Networks</li> <li>• Multimedia (Audio, Image and Video) Processing</li> <li>• Wireless and Mobile Systems</li> <li>• Network Applications</li> <li>• Automotive Applications</li> <li>• Financial Applications</li> <li>• Bioinformatics Applications</li> <li>• Biology Inspired Applications</li> </ul>	<ul style="list-style-type: none"> <li>• Configurable Systems-on-Chip</li> <li>• Energy Efficiency Issues</li> <li>• Devices and Circuits</li> <li>• Reconfiguration Techniques</li> <li>• High Level Design Methods</li> <li>• Languages and Compilers for Reconfigurable Computing Systems</li> <li>• System Support</li> <li>• Adaptive Runtime Support</li> <li>• Organic Computing</li> </ul>

## Submission Guidelines:

Authors should submit and register their paper through our web-interface which can be found at: <http://www.ece.lsu.edu/vaidy/raw/> The web interface will be accessible after October 1st, 2008.

All manuscripts will be reviewed by at least three members of the program committee. Submissions should be a complete manuscript (not to exceed 8 pages of single spaced text, including figures and tables) or, in special cases, may be a summary of relevant work. Submissions should be in pdf-format and will print on standard letter size paper (8.5" x 11").

IEEE CS Press will publish the IPDPS symposium and workshop abstracts as a printed volume. The complete symposium and workshop proceedings will also be published by IEEE CS Press as a CD-ROM disk.

## Important Dates:

Manuscript due:	October 31, 2008
Notification of acceptance:	January 15, 2009
Camera-ready Papers Due:	February 15, 2009

## Organization:

<b>Workshop Co-Chairs:</b>	Jürgen Becker, Karlsruhe Institute of Technology - KIT, Germany ( <a href="mailto:becker@kit.edu">becker@kit.edu</a> )  Philip Leong, Chinese University of Hong Kong ( <a href="mailto:phwl@cse.cuhk.edu.hk">phwl@cse.cuhk.edu.hk</a> )
<b>Program Co-Chairs:</b>	Ryan Kastner, UC San Diego, USA ( <a href="mailto:kastner@cs.ucsd.edu">kastner@cs.ucsd.edu</a> )  Koen Bertels, TU Delft, the Netherlands ( <a href="mailto:k.l.m.bertels@tudelft.nl">k.l.m.bertels@tudelft.nl</a> )
<b>Steering Chair:</b>	Viktor K. Prasanna, University of Southern California, USA ( <a href="mailto:prasanna@ganges.usc.edu">prasanna@ganges.usc.edu</a> )
<b>Publicity Chair (USA):</b>	Ramachandran Vaidyanathan, Louisiana State University, USA ( <a href="mailto:vaidy@ece.lsu.edu">vaidy@ece.lsu.edu</a> )
<b>Publicity Chair (Europe, Asia):</b>	Reiner Hartenstein, Kaiserslautern University of Technology, Germany ( <a href="mailto:reiner@hartenstein.de">reiner@hartenstein.de</a> )