



Workshop organized in the framework of the 2008 International Conference on High Performance Embedded Architectures & Compilers **HiPEAC 2008**

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Preliminary

Call For Papers - WRC 2008

2nd HiPEAC Workshop on

Reconfigurable Computing

January 27, 2008

Göteborg, Sweden

http://ce.et.tudelft.nl/HiPEACRC_WS/

The HiPEAC Workshop on Reconfigurable Computing provides a forum for researchers active in domains within the reconfigurable computing area. Its main focus is on reconfigurable **architectures, tools** that facilitate such architectures, and **applications** tailored for reconfigurable platforms. The workshop intends to bring together both hardware designers and software developers that make extensive use of reconfigurable computing. Moreover, it aims at enabling scientific discussions regarding future challenging issues.

The **topics of interest** include, but are not limited to:

Reconfigurable Architectures:

- Novel architectures (logic blocks, interconnects, I/O);
- Reconfigurable fabrics combined with dedicated system blocks (DSP, processors, memory etc.);
- Low power reconfigurable architectures;
- Networks on Chip tailored for reconfigurable architectures;
- Dynamic and run-time reconfiguration;
- Defect and Fault tolerance.

Reconfigurable Tools and Technologies:

- System level design and HW/SW co-design;
- Static and dynamic power efficiency;
- Modeling, optimization, technology mapping and design verification;
- Design and debug of reconfigurable systems;
- Testing, verification and benchmarking;
- Dedicated compilers and high-level languages.

Reconfigurable Applications and Algorithms:

- Adaptive and bio inspired applications;
- Application domain specific, e.g. multimedia, bioinformatics, cryptography and more;
- High-performance, high reliability and/or power efficient application acceleration;
- Rapid prototyping.

Authors are invited to electronically submit papers of up to 10 pages in [Springer LNCS format](#) in the following website: <http://www.easychair.org/HiPEACRC-WS-2008/>. There will be informal workshop proceedings for the participants, while selected papers will be extended for a special issue journal publication in Transactions on HiPEAC <http://www.hipeac.net/journal/>.

IMPORTANT DATES

Paper Submission Deadline:	November 2, 2007
Notification of acceptance:	December 10, 2007
Final version due:	December 24, 2007

This workshop is co-located with and followed by **HiPEAC 2008** (2008 International Conference on High Performance Embedded Architectures & Compilers, www.hipeac.net/conference/).